DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD17145(A1), 17147(A1), 17149(A1)

SMALL, GENERAL-PURPOSE 4-BIT SINGLE-CHIP MICROCONTROLLERS

The μPD17145(A1), 17147(A1), and 17149(A1) are 4-bit single-chip microcontrollers integrating an 8-bit A/D converter (4 channels), a timer function (3 channels), and a serial interface.

These microcontrollers employ a CPU of the general-purpose register type that can execute direct memory operations and direct memory-to-memory data transfer for efficient programming. All the instructions consist of 16 bits per word.

In addition, a one-time PROM version, the μPD17P149, is also available for program evaluation.

The functions of these microcontrollers are described in detail in the following User's Manual. Be sure to read the following manual when designing your system:

μPD17145 Subseries User's Manual: IEU-1383

FEATURES

• 17K architecture	: General-purpose register type
	: Instruction length fixed to 16 bits
• Program memory (ROM)	: μPD17145(A1) : 2 KB (1024 × 16 bits)
	: μPD17147(A1) : 4 KB (2048 × 16 bits)
	: μPD17149(A1) : 8 KB (4096 × 16 bits)
• Data memory (RAM)	: 110 × 4 bits
• External interrupt	: 1 (INT pin, with sense input)
• Instruction execution time	: 2 μs (at 8 MHz: ceramic oscillation)
• 8-bit A/D converter	: 4 channels, absolute accuracy: ±1.5 LSB MAX. (V_{DD} = 4.0 to 5.5 V)
• Timer	: 3 channels
• Serial interface	: 1 channel (clocked 3-wire)
• POC circuit (mask option)	
• Operating voltage	: V_{DD} = 2.7 to 5.5 V (at 400 kHz to 2 MHz)
	: V_{DD} = 4.5 to 5.5 V (at 400 kHz to 8 MHz)
• Operating temperature	: T_a = –40 to +110 ˚C

APPLICATIONS

Automotive electronics, etc.

Unless contextually excluded, references in this data sheet to the μPD17149 (A1) mean the μPD17145 (A1) and μPD17147 (A1).

The information in this document is subject to change without notice.

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Printed in Japan

ORDERING INFORMATION

Part Number	Package	Quality Grade
μPD17145CT(A1)-×××	28-pin plastic shrink DIP (400 mil)	Special
μPD17145GT(A1)-×××	28-pin plastic SOP (375 mil)	Special
μPD17147CT(A1)-×××	28-pin plastic shrink DIP (400 mil)	Special
μPD17147GT(A1)-×××	28-pin plastic SOP (375 mil)	Special
μPD17149CT(A1)-×××	28-pin plastic shrink DIP (400 mil)	Special
μPD17149GT(A1)-×××	28-pin plastic SOP (375 mil)	Special

Remark ××× indicates ROM code suffix.

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

FUNCTION LIST

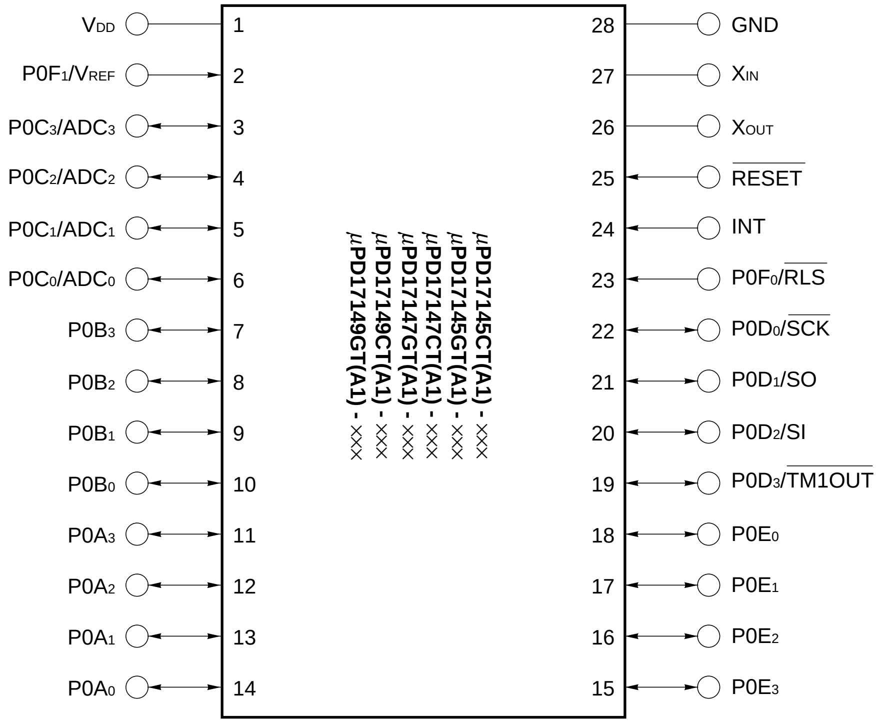
Part Number Item	μPD17145 (A1)	μPD17147 (A1)	μPD17149 (A1)
ROM capacity	2 KB (1024 × 16 bits)	4 KB (2048 × 16 bits)	8 KB (4096 × 16 bits)
RAM capacity	110 × 4 bits		
Stack	Address stack × 5, interrupt stack × 3		
I/O ports	23 { • I/O : 20 • Input : 2 • Sense input (INT pin[Note]) : 1		
A/D converter input	4 channels (shared with port pins), absolute accuracy: ±1.5 LSB MAX.		
Timer	3 channels { • 8-bit timer/counter: 2 channels (can be used as 1 channel of 16-bit timer) • 7-bit basic interval timer: 1 channel (can be used as watchdog timer)		
Serial interface	1 channel (3-wire)		
Interrupt	• Multiple interrupt by hardware (3 levels MAX.) • External interrupt (INT): 1 { Rising edge, falling edge, or both rising and falling edges selectable for detection. • Internal interrupt: 4 { • Timer 0 (TM0) • Timer 1 (TM1) • Basic interval timer (BTM) • Serial interface (SIO)		
Instruction execution time	2 μs (at 8 MHz, ceramic oscillation)		
Standby function	HALT, STOP		
POC circuit	Mask option (Can be used in application circuit that operates on V_{DD} = 5 V ± 10 %, 400 kHz to 4 MHz)		
Operating voltage	2.7 to 5.5 V (at 400 kHz to 2 MHz) 4.5 to 5.5 V (at 400 kHz to 8 MHz)		
Package	28-pin plastic shrink DIP (400 mil) 28-pin plastic SOP (375 mil)		
One-time PROM version	μPD17P149 (Quality grade is "standard" and not (A1). Operating temperature range: T_a = –40 to +85 °C)		

Note The INT pin is used as an input pin (sense input) when the external interrupt function is not used. The status of this pin is read by using the INT flag of a control register, not by a port register.

Caution The PROM version is functionally compatible with the mask ROM versions but its internal circuit and part of the electrical characteristics are different from those of the mask ROM versions. To replace the PROM version with a mask ROM version, thoroughly conduct application evaluation by using a sample of the mask ROM version.

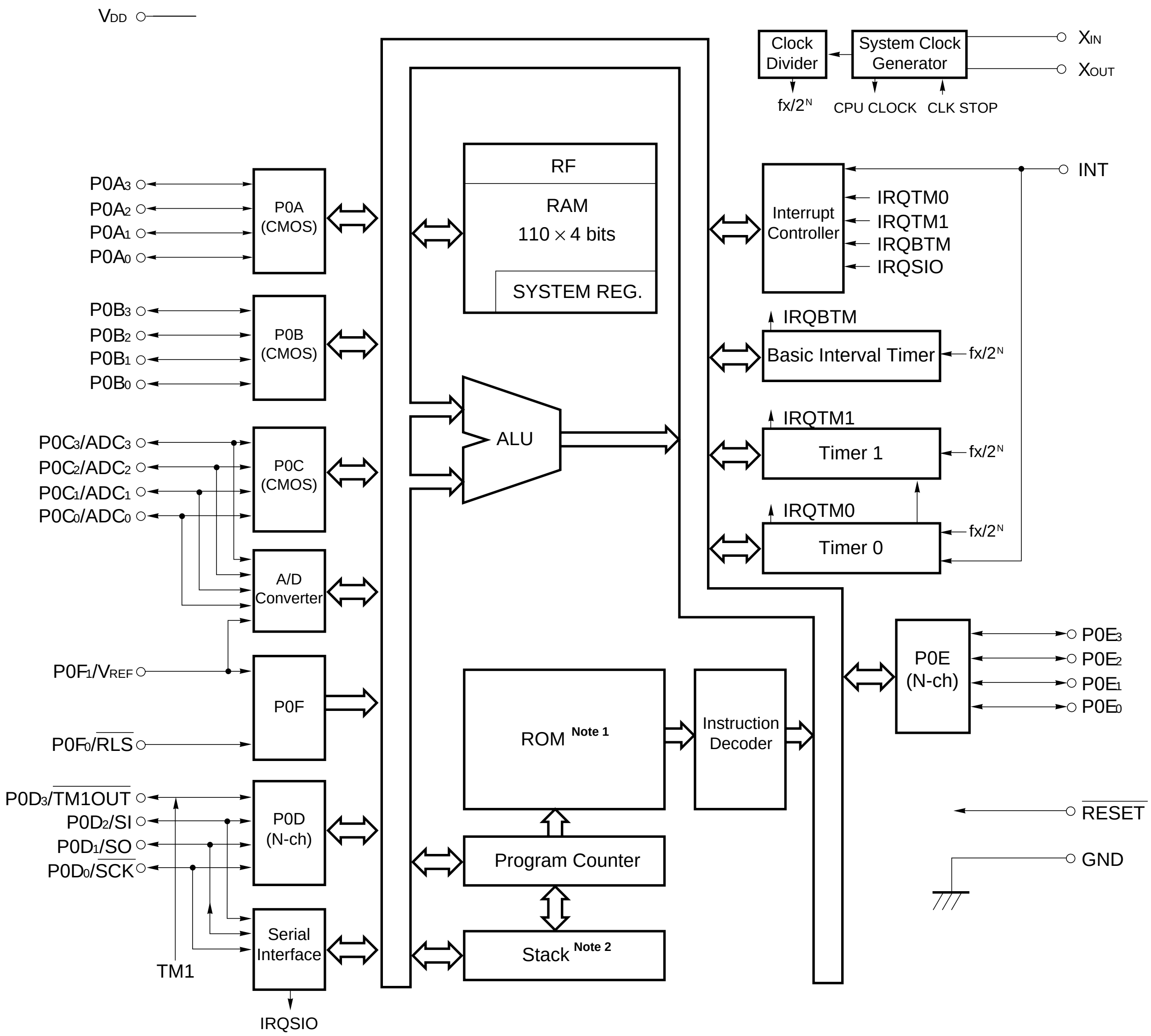
PIN CONFIGURATION (Top View)

28-pin plastic shrink DIP (400 mil)
28-pin plastic SOP (375 mil)



ADC_0-ADC_3	: analog input
GND	: ground
INT	: external interrupt input
$P0A_0$ to $P0A_3$	: port 0A
$P0B_0$ to $P0B_3$	: port 0B
$P0C_0$ to $P0C_3$	: port 0C
$P0D_0$ to $P0D_3$	: port 0D
$P0E_0$ to $P0E_3$	: port 0E
$P0F_0$ and $P0F_1$	: port 0F
$\overline{RESET}$	: reset input
$\overline{RLS}$	: standby release signal input
$\overline{SCK}$	: serial clock I/O
SI	: serial data input
SO	: serial data output
$\overline{TM1OUT}$	: timer 1 output
V_{DD}	: power
V_{REF}	: A/D converter reference voltage
X_{IN}, X_{OUT}	: for system clock oscillation

BLOCK DIAGRAM



Notes 1. The ROM capacity of each product is as follows:

1024 × 16 bits: μPD17145(A1)
2048 × 16 bits: μPD17147(A1)
4096 × 16 bits: μPD17149(A1)

2. The stack capacity of each product is as follows:

5 × 10 bits: μPD17145(A1)
5 × 11 bits: μPD17147(A1)
5 × 12 bits: μPD17149(A1)

Remark CMOS or N-ch in ( ) indicate the output format of the port.

CMOS : CMOS push-pull output
N-ch : N-ch open-drain output

CONTENTS

1. PIN

1.1. Pin Function

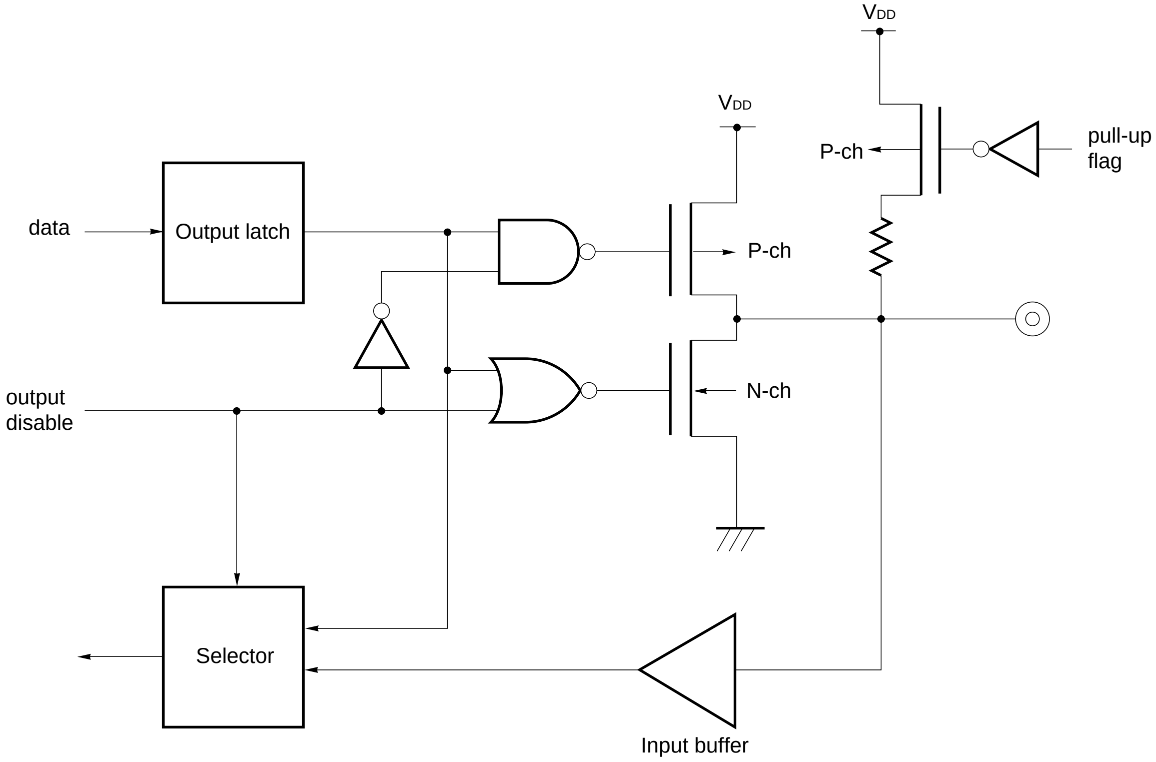
Pin Number	Symbol	Function	Output Format	After Reset
1	V$_{DD}$	Power supply.	—	—
2	P0F$_1$/V$_{REF}$	Reference voltage input to port 0F and A/D converter. • Pull-up resistor can be connected by mask option. • P0F$_1$ • Bit 1 of 2-bit input port (P0F) • V$_{REF}$ • Reference voltage input pin of A/D converter	Input	Input (P0F$_1$)
3 to 6	P0C$_3$/ADC$_3$ to P0C$_0$/ADC$_0$	Analog input to port 0C and A/D converter. • P0C$_3$-P0C$_0$ • 4-bit I/O port • Can be set in input or output mode bitwise. • ADC$_3$-ADC$_0$ • Analog inputs to A/D converter.	CMOS push-pull	Input (P0C)
7 8 9 10	P0B$_3$ P0B$_2$ P0B$_1$ P0B$_0$	Port 0B. • 4-bit I/O port • Can be set in input or output mode in 4-bit units. • Pull-up resistor can be connected in 4-bit units via software.	CMOS push-pull	Input
11 12 13 14	P0A$_3$ P0A$_2$ P0A$_1$ P0A$_0$	Port 0A. • 4-bit I/O port. • Can be set in input or output mode in 4-bit units. • Pull-up resistor can be connected in 4-bit units via software.	CMOS push-pull	Input
15 16 17 18	P0E$_3$ P0E$_2$ P0E$_1$ P0E$_0$	Port 0E. • 4-bit I/O port. • Can be set in input or output mode in 4-bit units. • Pull-up resistor can be connected in 4-bit units via software.	N-ch open-drain	Input
19 20 21 22	P0D$_3$/$\overline{\text{TM1OUT}}$ P0D$_2$/SI P0D$_1$/SO P0D$_0$/$\overline{\text{SCK}}$	Port 0D that is also used for timer 1 output, serial data input, serial data output, and serial clock I/O. • Pull-up resistor can be connected bitwise via software. • P0D$_3$-P0D$_0$ • 4-bit I/O port. • Can be set in input or output mode bitwise. • $\overline{\text{TM1OUT}}$ • Timer 1 output • SI • Serial data input • SO • Serial data output • $\overline{\text{SCK}}$ • Serial clock I/O	N-ch open-drain	Input (P0D)

Pin Number	Symbol	Function	Output Format	After Reset
23	P0F$_0$/$\overline{\text{RLS}}$	Port 0F or standby mode release signal input. • Pull-up resistor can be connected by mask option. • R0F$_0$ • Bit 0 of 2-bit input port (P0F) • $\overline{\text{RLS}}$ • Standby mode release signal input	Input	Input (P0F$_0$)
24	INT	External interrupt request signal input. Also used to release standby mode. • Pull-up resistor can be connected by mask option.	Input	Input
25	$\overline{\text{RESET}}$	System reset input. • Pull-up resistor can be connected by mask option.	Input	Input
26 27	X$_{\text{OUT}}$ X$_{\text{IN}}$	For system clock oscillation. Connect ceramic resonator across X$_{\text{IN}}$ and X$_{\text{OUT}}$.	—	—
28	GND	GND	—	—

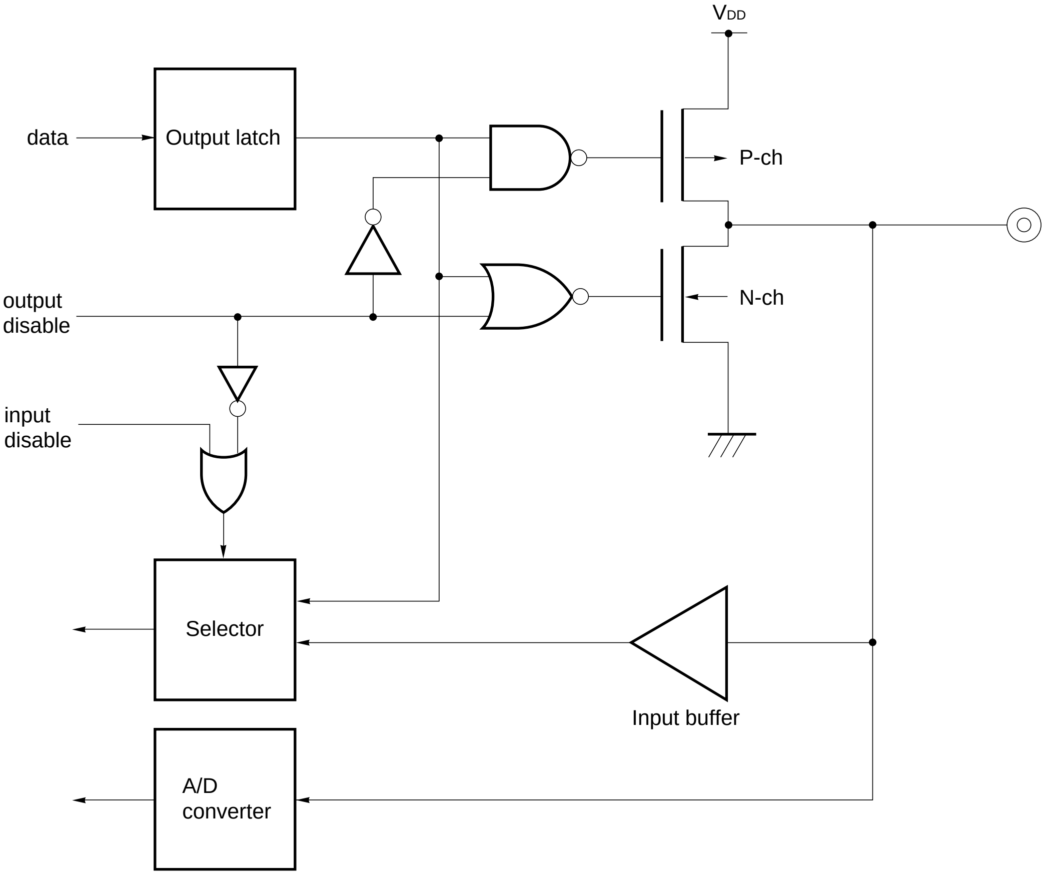
1.2 Equivalent Circuit of Pin

The input/output circuit of each pin is shown below, partially simplified.

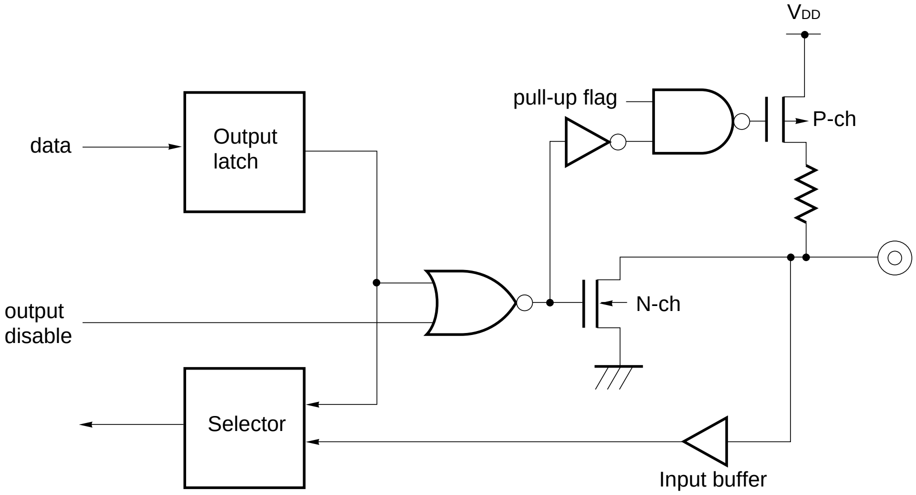
(1) $P0A_0$ to $P0A_3$ and $P0B_0$ to $P0B_3$



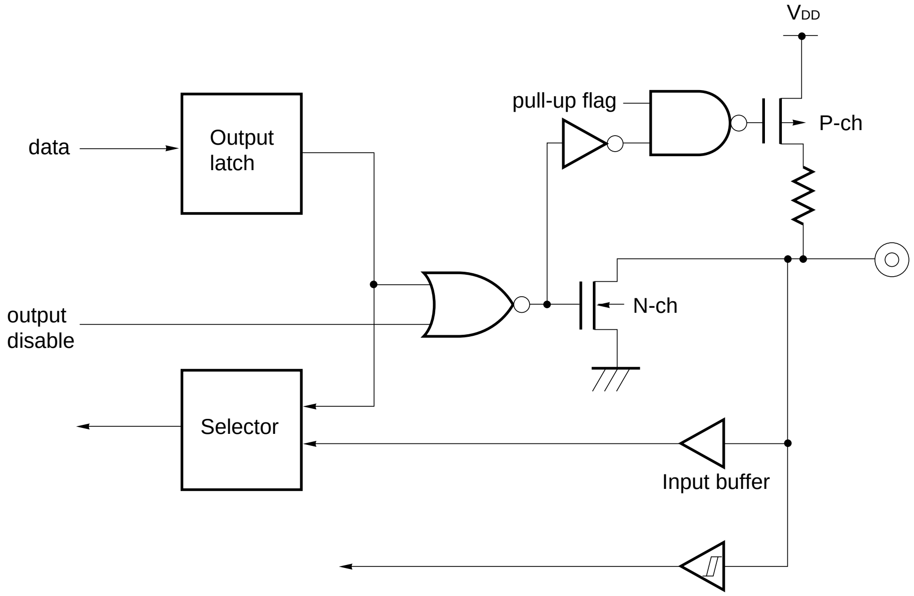
(2) P0C$_0$/ADC$_0$ to P0C$_3$/ADC$_3$



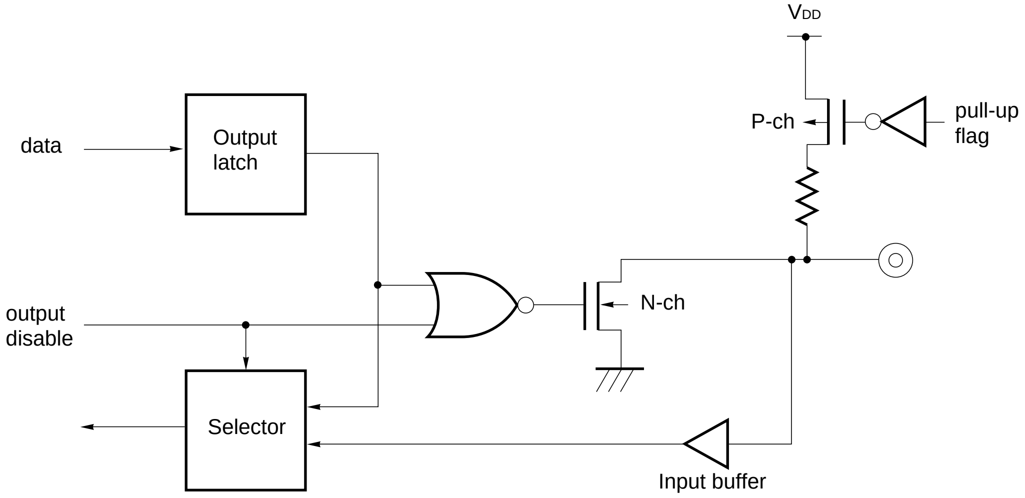
(3) P0D$_3$/$\overline{\text{TM1OUT}}$ and P0D$_1$/SO



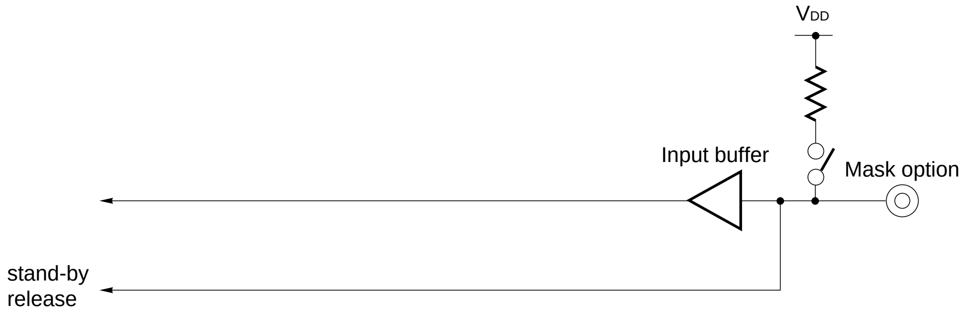
(4) P0D2/SI and P0D0/$\overline{\text{SCK}}$



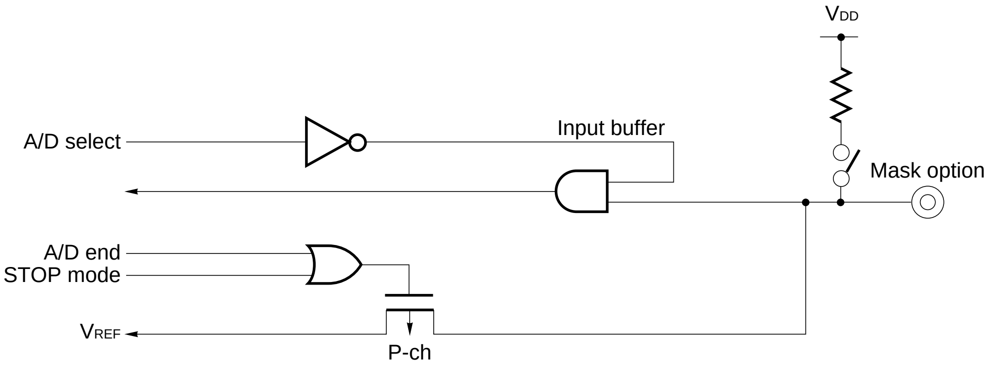
(5) P0E0 to P0E3



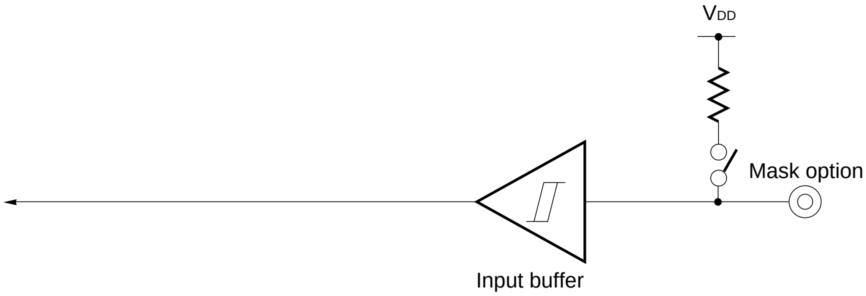
(6) P0F0/$\overline{\text{RLS}}$



(7) P0F$_1$/V$_{REF}$



(8) $\overline{\text{RESET}}$ and INT



1.3 Handling of Unused Pins

Handle unused pins as shown in the table below.

Table 1-1. Handling of Unused Pins

Pin Name			Handling	
			Internally	Externally
Port	Input mode	P0A, P0B, P0D, P0E	Connect on-chip pull-up resistor via software.	Open
		P0C	—	Connect to V_{DD} via pull-up resistor, or to GND via pull-down resistor[Note 1].
		P0F$_1$	Do not connect on-chip pull-up resistor by mask option.	Directly connect to V_{DD} or GND.
			Connect on-chip pull-up resistor by mask option.	Open
		P0F$_0$[Note 2]	Do not connect on-chip pull-up resistor by mask option.	Directly connect to GND.
	Output mode	P0A, P0B, P0C (CMOS port)	—	Open
		P0D (N-ch open-drain port)	Output low level.	
		P0E (N-ch open-drain port)	Do not connect pull-up on-chip resistor via software, but output low level.	
			Connect on-chip pull-up resistor via software and output high level.	
External interrupt (INT)			Do not connect on-chip pull-up resistor by mask option.	Directly connect to V_{DD} or GND.
			Connect on-chip pull-up resistor by mask option.	Open
$\overline{\text{RESET}}$[Note 3] (when only internal POC circuit is used)			Do not connect on-chip pull-up resistor by mask option.	Directly connect to V_{DD}.
			Connect on chip pull-up resistor by mask option.	

Notes 1. Take into consideration the drive capability and current dissipation of a port when the port is externally pulled up or down. To pull up or down the port with a high resistance, exercise care so that noise is not superimposed on the port pin. The appropriate value of the pull-up or pull-down resistor differs depending on the application circuit. Generally, select a resistor of several 10 kΩ.

2. The P0F$_0$/$\overline{\text{RLS}}$ pin is also used to set a test mode. When this pin is not used, do not connect a pull-up resistor to it by mask option, but directly connect it to GND.

3. In an application circuit where a high reliability is required, be sure to input the $\overline{\text{RESET}}$ signal from an external source. The $\overline{\text{RESET}}$ pin is also used to set a test mode. When this pin is not used, directly connect it to V_{DD}.

Caution It is recommended to fix the input/output mode, pull-up resistor by software, and the output level of the pin by repeatedly setting them in each loop of the program.

1.4 Note on Using $\overline{\text{RESET}}$ and P0F$_0$/$\overline{\text{RLS}}$ Pins

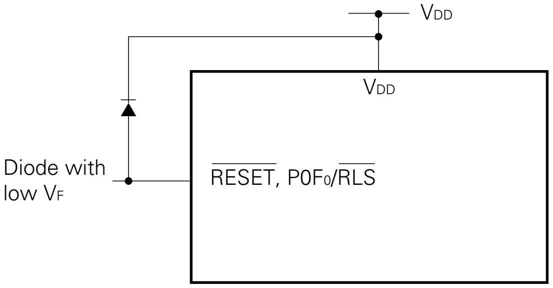
The $\overline{\text{RESET}}$ and P0F$_0$/$\overline{\text{RLS}}$ pins also have a function to set a test mode in which the internal operation of the μPD17149(A1) is tested (for IC test only), in addition to the function described in **1.1 Pin Function**.

If a voltage higher than V$_{DD}$ is applied to these pins, the test mode is set. If a noise higher than V$_{DD}$ is superimposed on these pins during normal operation, therefore, the test mode is set by mistake, affecting normal operation.

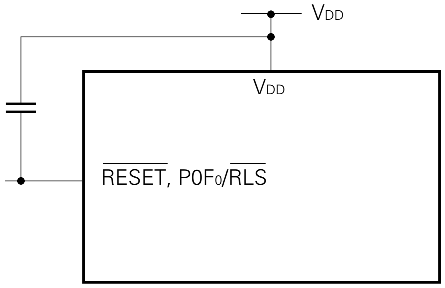
If the wiring length of the $\overline{\text{RESET}}$ or P0F$_0$/$\overline{\text{RLS}}$ pin is too long, for example, noise may be superimposed on the pin.

To prevent this, the wiring length must be kept as short as possible. Otherwise, use a diode or capacitor as shown below.

○ **Connect a low-V$_F$ diode between V$_{DD}$ and $\overline{\text{RESET}}$, P0F$_0$/$\overline{\text{RLS}}$**



○ **Connect a capacitor between V$_{DD}$ and $\overline{\text{RESET}}$, P0F$_0$/$\overline{\text{RLS}}$**



2. PROGRAM MEMORY (ROM)

Table 2-1 shows the program memory configuration of the μPD17145(A1), 17147(A1), and 17149(A1).

Table 2-1. Program Memory Configuration

Part Number	Program Memory Capacity	Program Memory Address
μPD17145(A1)	2 KB (1024 × 16 bits)	0000H-03FFH
μPD17147(A1)	4 KB (2048 × 16 bits)	0000H-07FFH
μPD17149(A1)	8 KB (4096 × 16 bits)	0000H-0FFFH

The program memory stores programs and constant data tables.

The program memory is addressed by the program counter.

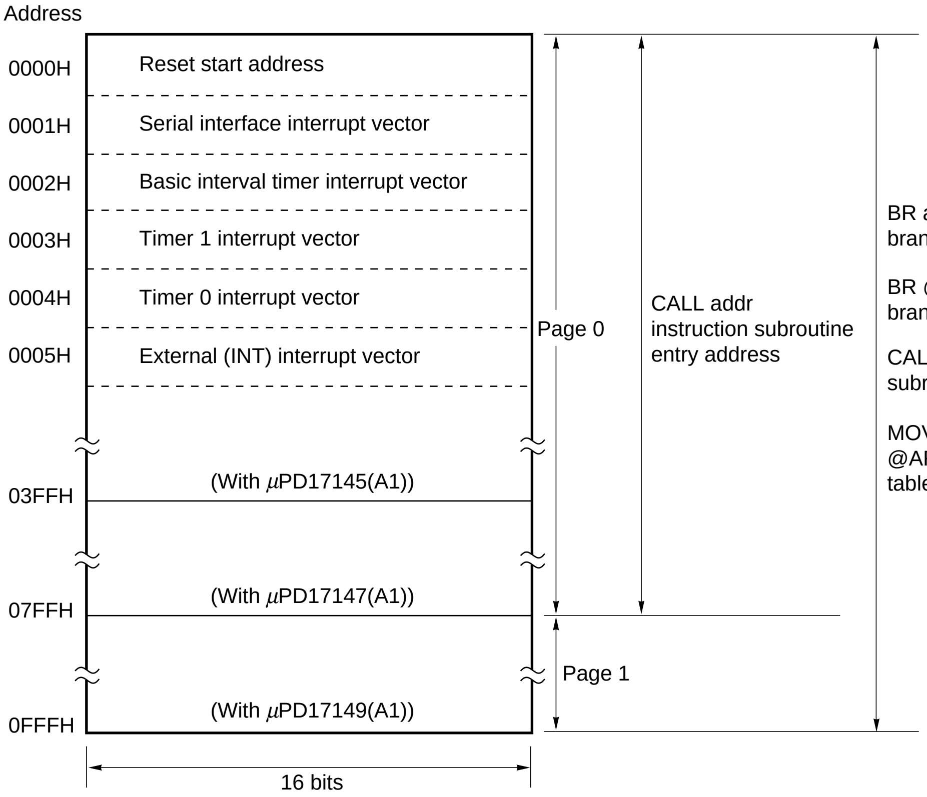
Addresses 0000H-0005H are allocated to a reset start address and various interrupt vector addresses.

2.1 Configuration of Program Memory

Figure 2-1 shows the program memory map. The program memory is divided in units called “pages” each of which consists of 2K steps with one step made up of 16 bits.

Addresses 0000H-07FFH (page 0) of the program memory can be specified by the direct subroutine call instruction. The entire address range of the program memory, 0000H-0FFFH, can be specified by the branch, indirect subroutine call, and table reference instructions.

Figure 2-1. Program Memory Map



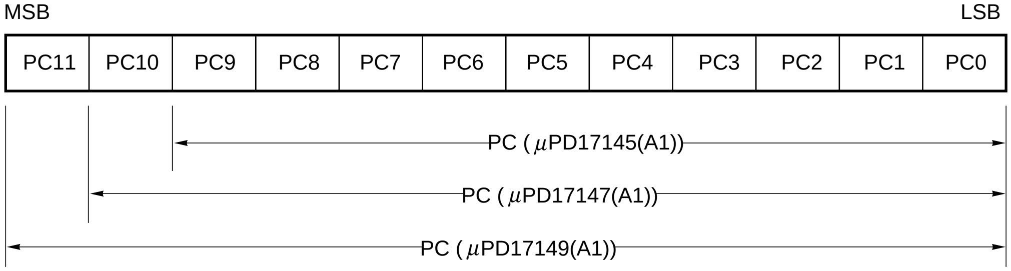
3. PROGRAM COUNTER (PC)

The program counter is used to address the program memory.

3.1 Configuration of Program Counter

The program counter is a 10-/11-/12-bit binary counter as shown in Figure 3-1.

Figure 3-1. Program Counter



3.2 Operation of Program Counter

Usually, the contents of the program counter are automatically incremented each time an instruction has been executed. When reset has been effected, when a branch, subroutine call, return, or table reference instruction has been executed, or when an interrupt has been acknowledged, the address of the program memory to be executed next is set to the program counter.

Figure 3-2. Value of Program Counter after Instruction Execution

Bit of Program Counter	Value of Program Counter											
Instruction	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
At reset	0	0	0	0	0	0	0	0	0	0	0	0
BR addr	0	Value specified by addr										
	1											
CALL addr	0											
BR @AR CALL @AR (MOVT DBF, @AR)	Contents of address register (AR)											
RET RETSK RETI	Contents of address stack indicated by stack pointer (return address)											
When interrupt is acknowledged	Vector address of each interrupt											

Remark The μPD17145(A1) does not have PC11 and PC10. The μPD17147(A1) does not have PC11.

4. STACK

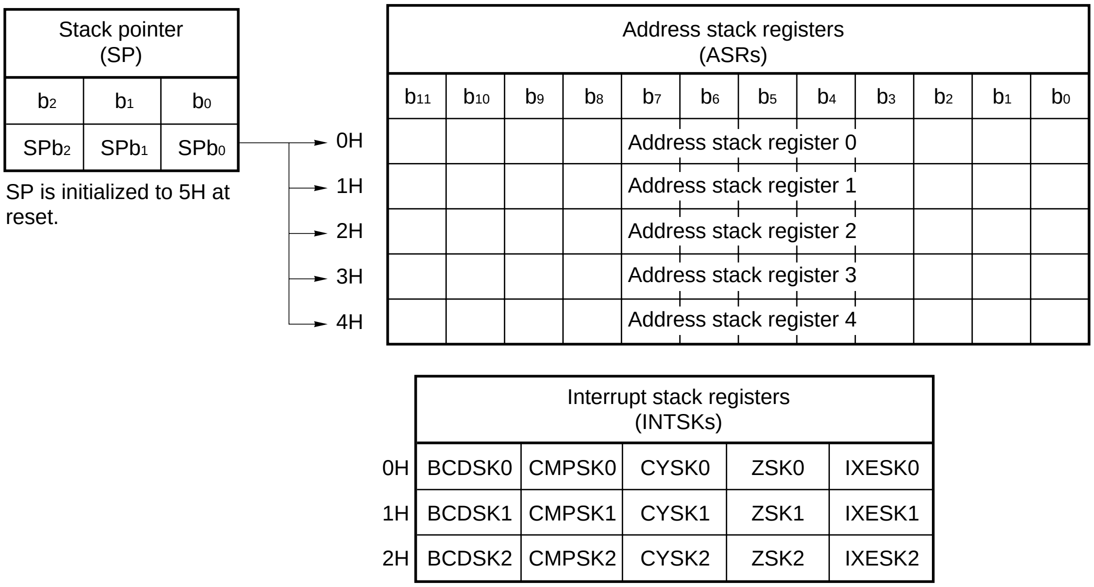
The stack is a register to which the return address of the program or the contents of the system registers, which are described later, are saved when a subroutine call instruction is executed or when an interrupt is acknowledged.

4.1 Configuration of Stack

Figure 4-1 shows the configuration of the stack.

The stack consists of a 3-bit binary counter, stack pointer (SP), five 10-bit (μPD17145(A1)), 11-bit (μPD17147(A1)), or 12-bit (μPD17149(A1)) address stack registers (ASRs), and three 5-bit interrupt stack registers (INTSKs).

Figure 4-1. Configuration of Stack



	Interrupt stack registers (INTSKs)				
0H	BCDSK0	CMPSK0	CYSK0	ZSK0	IXESK0
1H	BCDSK1	CMPSK1	CYSK1	ZSK1	IXESK1
2H	BCDSK2	CMPSK2	CYSK2	ZSK2	IXESK2

4.2 Stack Function

The stack is used to save a return address when the subroutine call or table reference instruction is executed. When an interrupt is acknowledged, the return address of the program and the contents of the program status word (PSWORD) are automatically saved to the stack. After they are saved to the stack, all the bits of PSWORD are cleared to 0.

5. DATA MEMORY (RAM)

The data memory is used to store data for operation and control. Data can always be written to or read from this memory by using an instruction.

5.1 Configuration of Data Memory

The data memory is assigned addresses each consisting of 7 bits. The higher 3 bits of an address are called a “row address”, while the lower 4 bits are called a “column address”.

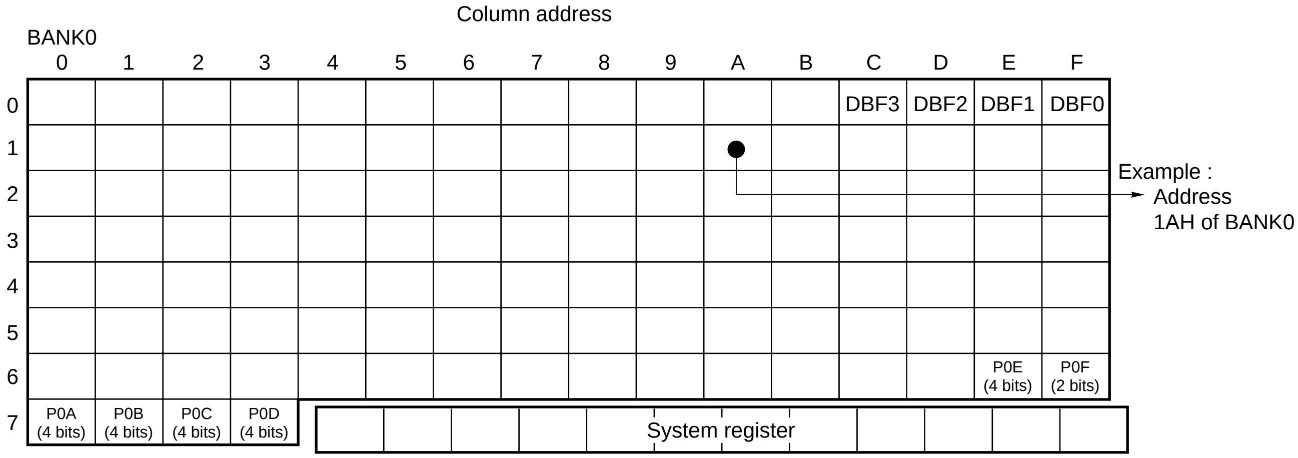
Take address 1AH for example. The row address of this address is 1H and the column address is 0AH.

One address consists of 4 bits (= 1 nibble) of memory.

The data memory consists of an area to which the user can save data, and areas to which special functions are allocated in advance. These areas are:

• System register (SYSREG)	(Refer to 7. SYSTEM REGISTER (SYSREG).)
• Data buffer (DBF)	(Refer to 9. DATA BUFFER (DBF).)
• Port register	(Refer to 11. PORT.)

Figure 5-1. Configuration of Data Memory



6. GENERAL REGISTER (GR)

As its name implies, the general register is used for general purposes such as data transfer and operation.

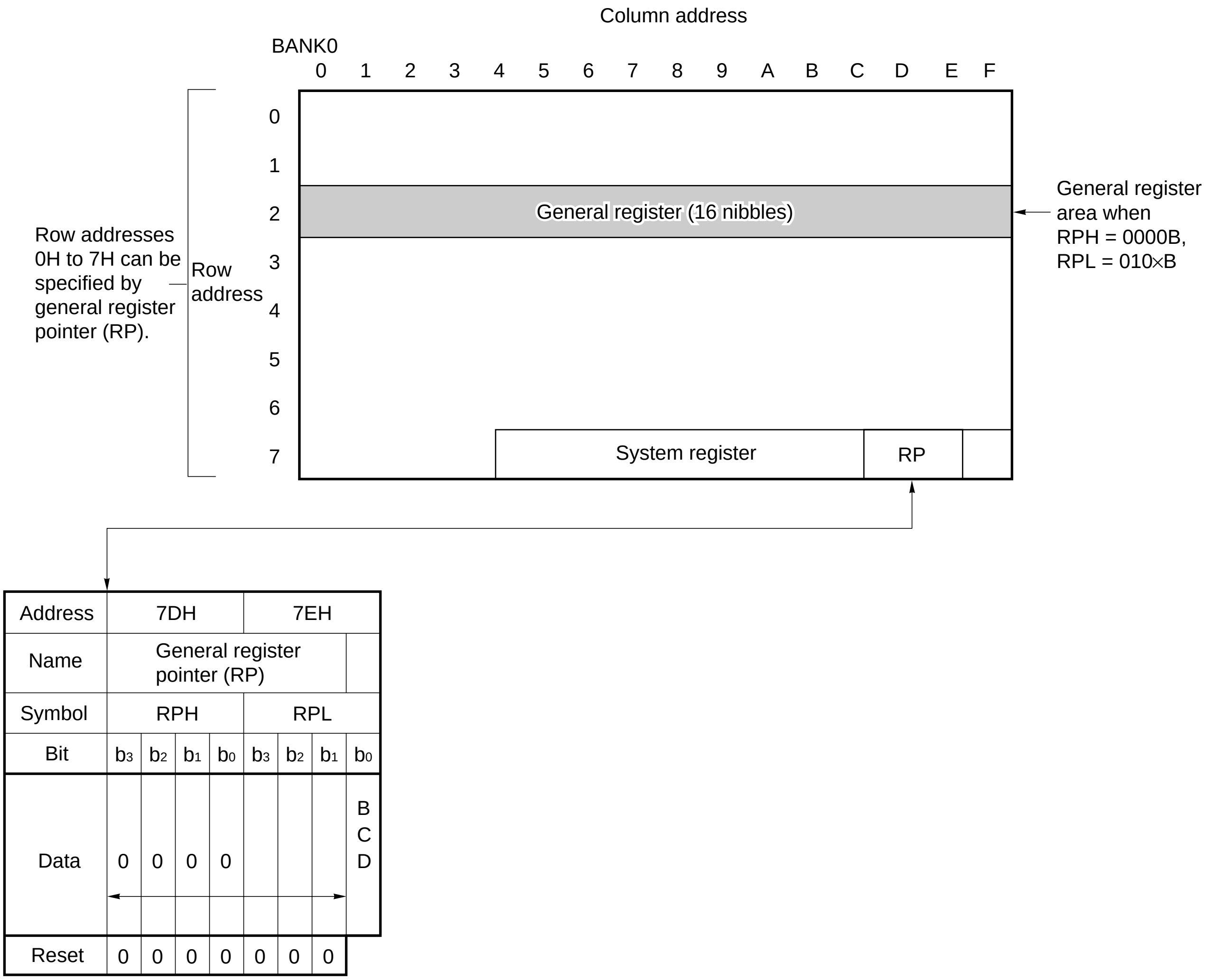
The general register of the 17K series is not a fixed area, but an area specified on the data memory by using the general register pointer (RP). Therefore, a part of the data memory area can be specified as a general register as necessary, so that data can be transferred between data memory areas and the data in the data memory can be operated with a single instruction.

6.1 General Register Pointer (RP)

RP is a pointer that specifies part of the data memory as the general register. RP specifies the bank and row addresses of a data memory area that is to be specified as the general register. Consisting of a total of 7 bits, RP is assigned to 7DH (RPH) and 7EH (RPL), and the higher 3 bits of the system register (refer to **7. SYSTEM REGISTER (SYSREG)**).

RPH specifies a bank, and RPL specifies a data memory row address.

Figure 6-1. Configuration of General Register Pointer


Column address
BANK0
0 1 2 3 4 5 6 7 8 9 A B C D E F
0
1
2
3
4
5
6
7
General register (16 nibbles)
General register area when RPH = 0000B, RPL = 010×B
Row addresses 0H to 7H can be specified by general register pointer (RP).
Row address
System register
RP

Address	7DH				7EH			
Name	General register pointer (RP)							
Symbol	RPH				RPL			
Bit	b_3	b_2	b_1	b_0	b_3	b_2	b_1	b_0
Data	0	0	0	0				B C D
Reset	0	0	0	0	0	0	0	

7. SYSTEM REGISTER (SYSREG)

The system register (SYSREG) is a register that directly controls the CPU, and is located on the data memory.

7.1 Configuration of System Register

Figure 7-1 shows the location of the system register on the data memory. As shown in this figure, the system register is located at addresses 74H-7FH of the data memory.

Because the system register is located on the data memory, it can be manipulated by all the data memory manipulation instructions. It is therefore possible to specify the system register as a general register.

Figure 7-1. Location of System Register on Data Memory

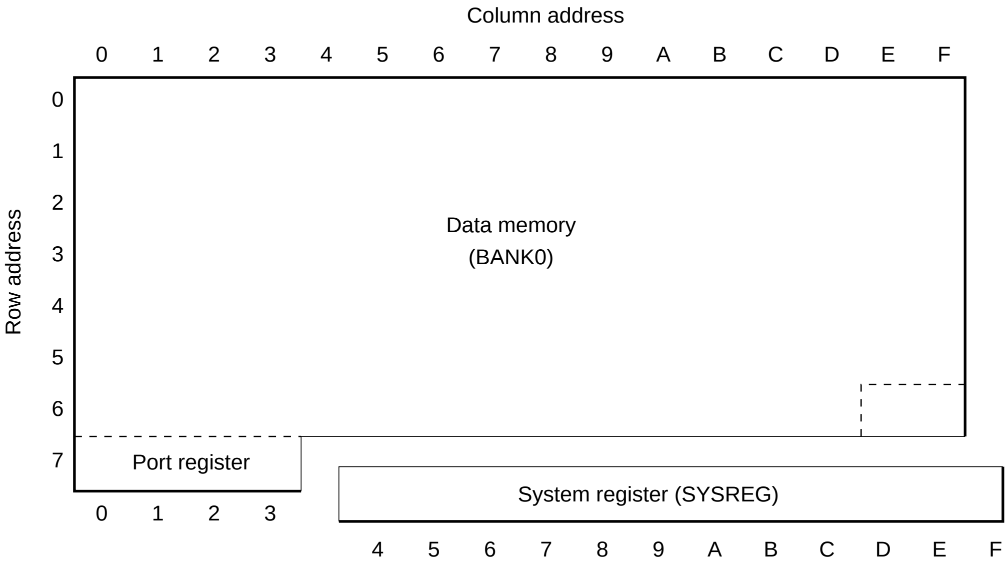


Figure 7-2 shows the configuration of the system register. As shown in this figure, the system register consists of the following seven registers:

• Address register	(AR)
• Window register	(WR)
• Bank register	(BANK)
• Index register	(IX)
• Data memory row address pointer	(MP)
• General register pointer	(RP)
• Program status word	(PSWORD)

Figure 7-2. Configuration of System Register

Address	74H				75H				76H				77H				78H				79H				7AH				7BH				7CH				7DH				7EH				7FH			
Name	Address register (AR)																Window register (WR)				Bank register (BANK)				Index register (IX) Data memory row address pointer (MP)												General register pointer (RP)							Program status word (PSWORD)				
Symbol	AR3				AR2				AR1				AR0				WR				BANK				IXH MPH				IXM MPL				IXL				RPH				RPL				PSW			
Bit	b_3	b_2	b_1	b_0	b_3	b_2	b_1	b_0	b_3	b_2	b_1	b_0	b_3	b_2	b_1	b_0	b_3	b_2	b_1	b_0	b_3	b_2	b_1	b_0	b_3	b_2	b_1	b_0	b_3	b_2	b_1	b_0	b_3	b_2	b_1	b_0	b_3	b_2	b_1	b_0	b_3	b_2	b_1	b_0	b_3	b_2	b_1	b_0
																										(IX)																						
Data[Note1]	0	0	0	0	[Note2]																0	0	0	0	MPE	0	0	0	0								0	0	0	0				BCD	CMP	CY	Z	IXE
	(AR)																				(BANK)					(MP)											(RP)											
Initial value at reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Undefined				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Notes 1. 0 in this field means that the bit is “fixed to 0”.

2. b_3 and b_2 of AR2 of the μPD17145(A1) are fixed to 0. b_3 of AR2 of the μPD17147(A1) is fixed to 0.

8. REGISTER FILE (RF)

The register file is a register that mainly sets the conditions of the peripheral hardware.

8.1 Configuration of Register File

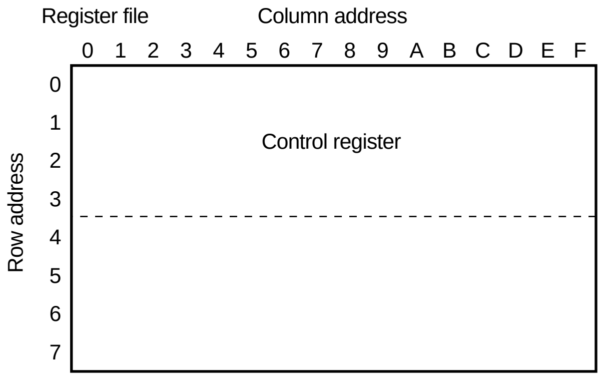
8.1.1 Configuration of register file

Figure 8-1 shows the configuration of the register file.

As shown in this figure, the register file consists of 128 nibbles (128 × 4 bits). Like the data memory, the register file is assigned addresses in 4-bit units, with row addresses 0H-7H and column addresses 0H-0FH.

Addresses 00H-3FH of the register file are called a control register.

Figure 8-1. Configuration of Register File



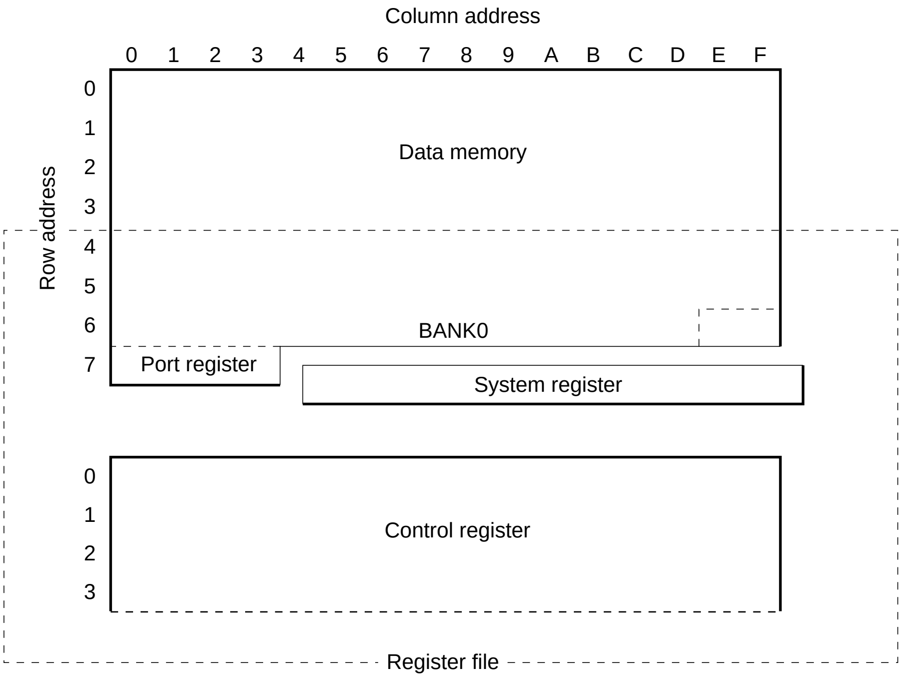
8.1.2 Register file and data memory

Figure 8-2 shows the relationships between the register file and data memory.

As shown in this figure, addresses 40H to 7FH of the register file overlaps the data memory.

It seems from the program as if addresses 40H to 7FH of the data memory exist at addresses 40H-7FH of the register file.

Figure 8-2. Relationships between Register File and Data Memory



8.2 Function of Register File

8.2.1 Function of register file

The register file is a collection of registers that set the conditions of the peripheral hardware by using the PEEK or POKE instruction.

The registers that control the peripheral hardware are allocated to addresses 00H-3FH. These registers are called control registers.

Addresses 40H-7FH of the register file overlap the ordinary data memory. These addresses can therefore be read or written by not only the MOV instruction but also the PEEK and POKE instructions.

8.2.2 Functions of control registers

The control registers are used to set the conditions of the peripheral hardware listed below.

For the details of the peripheral hardware and control registers, refer to the description of each peripheral hardware.

- Port
- 8-bit timers/counters (TM0, TM1)
- Basic interval timer (BTM)
- A/D converter
- Serial interface (SIO)
- Interrupt function
- Stack pointer (SP)

9. DATA BUFFER (DBF)

The data buffer consists of 4 nibbles allocated to addresses 0CH-0FH of BANK0 of the data memory.

This area is a data storage area that transfers data with the peripheral hardware of the CPU (address register, serial interface, timers 0 and 1, and A/D converter) by using the GET or PUT instruction. Moreover, the constants on the program memory can be read to the data buffer by using the MOVT DBF, @AR instruction.

9.1 Configuration of Data Buffer

Figure 9-1 shows the location of the data buffer on the data memory.

As shown in this figure, the data buffer is allocated addresses 0CH-0FH of the data memory, and consists of a total of 16 bits or 4 nibbles (4 × 4 bits).

Figure 9-1. Location of Data Buffer

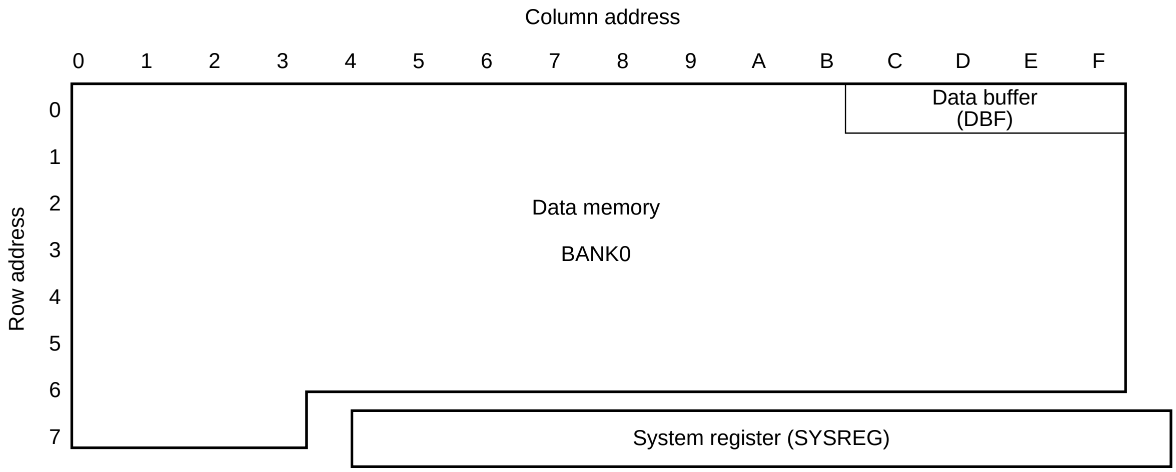


Figure 9-2 shows the configuration of the data buffer. As shown in this figure, the data buffer consists of 16 bits of the data memory, with the bit 0 of address 0FH as the LSB and bit 3 of address 0CH as the MSB.

Figure 9-2. Configuration of Data Buffer

Data memory BANK0	Address	0CH				0DH				0EH				0FH			
	Bit	b_3	b_2	b_1	b_0	b_3	b_2	b_1	b_0	b_3	b_2	b_1	b_0	b_3	b_2	b_1	b_0
Data buffer	Bit	b_{15}	b_{14}	b_{13}	b_{12}	b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
	Symbol	DBF3				DBF2				DBF1				DBF0			
	Data	MSB				Data											LSB

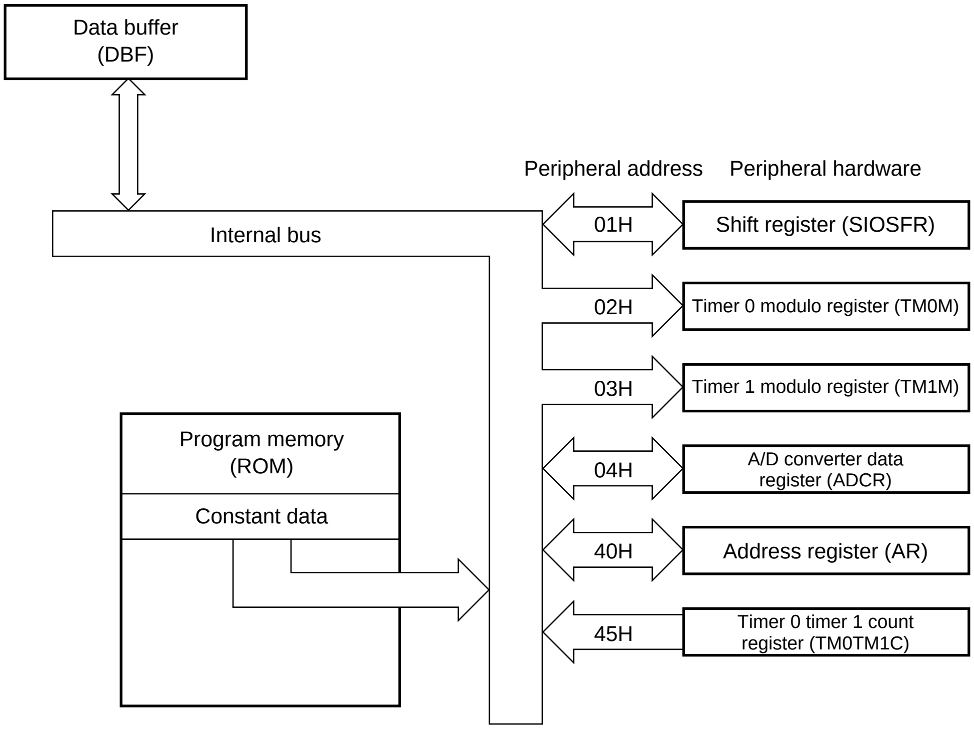
Because the data buffer is located on the data memory, it can be manipulated by all the data memory manipulation instructions.

9.2 Function of Data Buffer

The data buffer has two main functions.

One is to transfer data with the peripheral hardware, and the other is to read the constant data on the program memory (table reference). Figure 9-3 shows the relationships between the data buffer and peripheral hardware.

Figure 9-3. Data Buffer and Peripheral Hardware



10. ALU BLOCK

The ALU executes arithmetic and logical operations, bit judgment, and rotation processing of 4-bit data.

10.1 Configuration of ALU Block

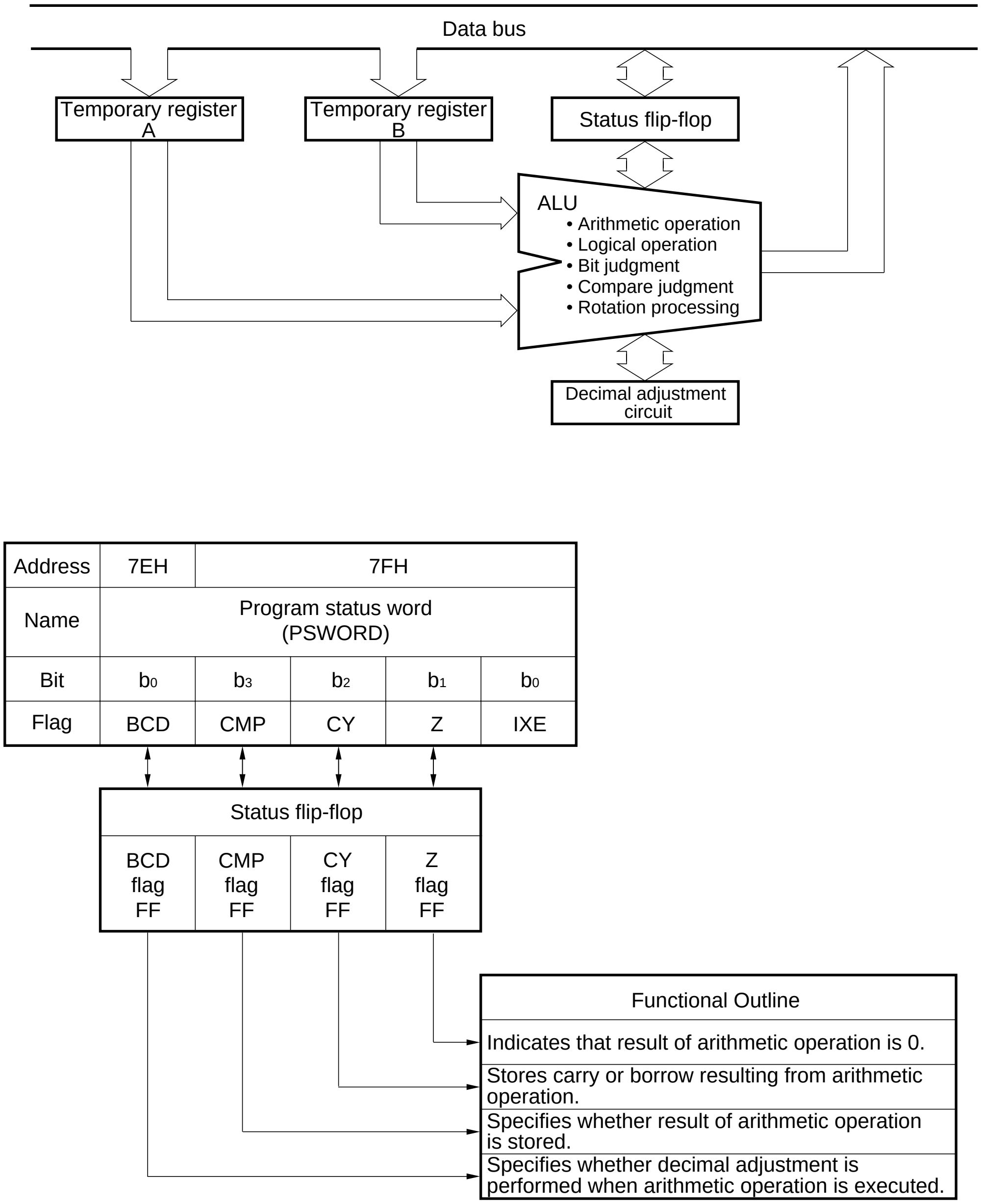
Figure 10-1 shows the configuration of the ALU block.

As shown, the ALU block consists of an ALU that processes 4-bit data, and peripheral circuits such as temporary registers A and B, status flip-flops that control the status of the ALU, and a decimal adjustment circuit that is used when a BCD operation is performed.

The status flip-flops are a zero flag FF, carry flag FF, compare flag FF, and BCD flag FF, as shown in Figure 10-1.

The status flip-flops correspond to the zero flag (Z), carry flag (CY), compare flag (CMP), and BCD flag (BCD) of the program status word (PSWORD: addresses 7EH, 7FH) on a one-to-one basis.

Figure 10-1. Configuration of ALU Block



Address	7EH	7FH			
Name	Program status word (PSWORD)				
Bit	b_0	b_3	b_2	b_1	b_0
Flag	BCD	CMP	CY	Z	IXE

Status flip-flop			
BCD flag FF	CMP flag FF	CY flag FF	Z flag FF

Functional Outline
Indicates that result of arithmetic operation is 0.
Stores carry or borrow resulting from arithmetic operation.
Specifies whether result of arithmetic operation is stored.
Specifies whether decimal adjustment is performed when arithmetic operation is executed.

11. PORTS

11.1 Port 0A ($P0A_0$, $P0A_1$, $P0A_2$, $P0A_3$)

Port 0A is a 4-bit I/O port with an output latch. It is mapped at address 70H of BANK0 of the data memory. The output format is CMOS push-pull output.

This port can be set in the input or output mode in 4-bit units. The input or output mode is specified by P0AGIO (bit 0 of address 2CH) on the register file.

When P0AGIO = 0, all the pins of port 0A are set in the input mode. When an instruction that reads the data of the port register is executed at this time, the pin status is read.

When P0AGIO = 1, all the pins of port 0A are set in the output mode, and the contents written to the output latch are output to the pins. When an instruction that reads the port status is executed with the port set in the output mode, the contents of the output latch, instead of the pin status, are read.

A pull-up resistor can be connected on-chip to this port through software. Whether the pull-up resistor is connected is specified by P0AGPU (bit 0 at address 0CH) of the register file. All the four pins are pulled up when P0AGPU = 1. When P0AGPU = 0, the pull-up resistor is not connected.

P0AGIO and P0AGPU are cleared to “0” at reset, and all the P0A pins are set in the input mode without the pull-up resistor connected. The value of the output latch is also cleared to “0”.

Table 11-1. Writing and Reading Port Register (0.70H)

P0AGIO	Input/Output	BANK0 70H	
RF: 2CH, bit 0	Mode of Pin	Write	Read
0	Input	Enabled Write to P0A latch	P0A pin status
1	Output		P0A latch contents

11.2 Port 0B (P0B$_0$, P0B$_1$, P0B$_2$, P0B$_3$)

Port 0B is a 4-bit I/O port with an output latch. It is mapped at address 71H of BANK0 of the data memory. The output format is CMOS push-pull output.

This port can be set in the input or output mode in 4-bit units. The input or output mode is specified by P0BGIO (bit 1 of address 2CH) on the register file.

When P0BGIO = 0, all the pins of port 0B are set in the input mode. When an instruction that reads the data of the port register is executed at this time, the pin status is read.

When P0BGIO = 1, all the pins of port 0B are set in the output mode, and the contents written to the output latch are output to the pins. When an instruction that reads the port status is executed with the port set in the output mode, the contents of the output latch, instead of the pin status, are read.

A pull-up resistor can be connected on-chip to this port through software. Whether the pull-up resistor is connected is specified by P0BGPU (bit 1 at address 0CH) of the register file. All the four-bit pins are pulled up when P0BGPU = 1. When P0BGPU = 0, the pull-up resistor is not connected.

P0BGIO and P0BGPU are cleared to “0” at reset, and all the P0B pins are set in the input mode without the pull-up resistor connected. The value of the output latch is also cleared to “0”.

Table 11-2. Writing and Reading Port Register (0.71H)

P0BGIO	Input/Output	BANK0 71H	
RF: 2CH, bit 1	Mode of Pin	Write	Read
0	Input	Enabled Write to P0B latch	P0B pin status
1	Output		P0B latch contents

11.3 Port 0C (P0C$_0$/ADC$_0$, P0C$_1$/ADC$_1$, P0C$_2$/ADC$_2$, P0C$_3$/ADC$_3$)

Port 0C is a 4-bit I/O port with an output latch. It is mapped at address 72H of BANK0 of the data memory. The output format is CMOS push-pull output.

This port can be set in the input or output mode in 1-bit units. The input or output mode is specified by P0CBIO0-P0CBIO3 (address 1CH) on the register file.

When P0CBIOn = 0 (n = 0 to 3), the corresponding port pin, P0Cn, is set in the input mode. When an instruction that reads the data of the port register is executed at this time, the pin status is read. When P0CBIOn = 1 (n = 0 to 3), the P0Cn pin is set in the output mode, and the contents written to the output latch are output to the pin. When an instruction that reads the port status is executed with a port pin set in the output mode, the contents of the output latch, instead of the pin status, are read.

At reset, P0CBIO0-P0CBIO3 are cleared to “0”, setting all the P0C pins in the input mode. The contents of the output latch are also cleared to “0” at this time.

Port 0C is also used to input analog voltages to the A/D converter. Whether each pin of the port is used as a port pin or analog input pin is specified by P0C0IDI-P0C3IDI (address 1BH) on the register file.

When P0CnIDI = 0 (n = 0-3), the P0C$_n$/ADC$_n$ pin functions as a port pin. When P0CnIDI = 1 (n = 0 to 3), the P0C$_n$/ADC$_n$ pin functions as an analog input pin of the A/D converter. If any of the P0CnIDI (n = 0 to 3) bits is set to “1”, the P0F$_1$/V$_{REF}$ pin is used as the V$_{REF}$ pin.

When a pin of port 0C is used as an analog input pin of the A/D converter, set the P0CnIDI corresponding to the pin to which an analog voltage is applied to 1, to disable the port input function. Moreover, clear P0CBIOn (n = 0-3) to 0 to set the input port mode. The pin used as an analog input pin is selected by ADCCH0 and ADCCH1 (bits 1 and 0 of address 22H) on the register file.

At reset, P0CBIO0-P0CBIO3, P0C0IDI-P0C3IDI, ADCCH0, and ADCCH1 are cleared to 0, setting the input port mode.

Table 11-3. Selecting Port or A/D Converter Mode

(n = 0 to 3)

P0CnIDI RF:1BH	P0CBIOn RF:1CH	Function	BANK0 72H	
			Write	Read
0	0	Input port	Enabled. P0C latch	Pin status
	1	Port output	Enabled. P0C latch	Contents of P0C latch
1	0	Analog input of A/D[Note 1]	Enabled. P0C latch	Contents of P0C latch
	1	Output port and analog input of A/D[Note 2]	Enabled. P0C latch	Contents of P0C latch

Notes 1. Normal setting when the P0C pins are used as the analog input pins of the A/D converter.

2. The P0C pins function as output port pins. At this time, the analog input voltages change with the output from the port. To use the pins as analog input pins, be sure to clear P0CBIOn to 0.

11.4 Port 0D (P0D$_0$/$\overline{\text{SCK}}$, P0D$_1$/SO, P0D$_2$/SI, P0D$_3$/$\overline{\text{TM1OUT}}$)

Port 0D is a 4-bit I/O port with an output latch. It is mapped at address 73H of BANK0 of the data memory. The output format is N-ch open-drain output.

This port can be set in the input or output mode in 1-bit units. The input or output mode is specified by P0DBIO0-P0DBIO3 (address 2BH) on the register file.

When P0DBIOn = 0 (n = 0 to 3), the corresponding port pin, P0Dn, is set in the input mode. When an instruction that reads the data of the port register is executed at this time, the pin status is read. When P0DBIOn = 1, the P0Dn pin is set in the output mode, and the contents written to the output latch are output to the pin. When an instruction that reads the port status is executed with a port pin set in the output mode, the contents of the output latch, instead of the pin status, are read.

A pull-up resistor can be connected on-chip to this port through software. Whether the pull-up resistor is connected or not is specified bitwise by using P0DBPU0-P0DBPU3 (address 0DH) on the register file. When P0DBPUn = 1, the P0Dn pin is pulled up. When P0DBPUn = 0, the pull-up resistor is not connected.

At reset, P0DBIOn is cleared to “0”, setting all the P0D pins in the input mode. The contents of the output latch are also cleared to “0” at this time. Note that the contents of the output latch are not changed even if the status of P0DBIOn is changed from “1” to “0”.

Port 0D is also used as serial interface input/output and timer 1 output pins. Whether the P0D$_0$ to P0D$_2$ pins are used as port pins or serial interface I/O pins ($\overline{\text{SCK}}$, SO, and SI) is specified by SIOEN (bit 0 of 0BH) on the register file. Whether the P0D$_3$ pin is used as a port pin or timer 1 output ($\overline{\text{TM1OUT}}$) pin is specified by TM1OSEL (bit 3 of 0BH) on the register file. If TM1OSEL = 1, “1” is output when timer 1 is reset, and the output is inverted each time the count value of timer 1 coincides with the contents of the modulo register.

Table 11-4. Contents of Register File and Pin Function

(n = 0 to 3)

Value of Register File			Pin Function			
TM1OSEL RF: 0BH Bit 3	SIOEN RF: 0BH Bit 0	P0DBIOn RF: 2BH Bit n	P0D$_0$/$\overline{\text{SCK}}$	P0D$_1$/SO	P0D$_2$/SI	P0D$_3$/$\overline{\text{TM1OUT}}$
0	0	0	Input port			
		1	Output port			
	1	0	$\overline{\text{SCK}}$	SO	SI	Input port
		1				Output port
1	0	0	Input port			$\overline{\text{TM1OUT}}$
		1	Output port			
	1	0	$\overline{\text{SCK}}$	SO	SI	
		1				

Table 11-5. Read Contents of Port Register (0.73H)

Port Mode		Read Contents of Port Register (0.73H)
Input port		Pin status
Output port		Contents of output latch
$\overline{\text{SCK}}$	Internal clock selected as serial clock	Contents of output latch
	External clock selected as serial clock	Pin status
SI		Pin status
SO		Contents of output latch
$\overline{\text{TM1OUT}}$		Contents of output latch

11.5 Port 0E ($P0E_0$, $P0E_1$, $P0E_2$, $P0E_3$)

Port 0E is a 4-bit I/O port with an output latch. It is mapped at address 6EH of BANK0 of the data memory. The output format is N-ch open-drain output.

This port can be set in the input or output mode in 4-bit units. The input or output mode is specified by P0EGIO (bit 2 of address 2CH) on the register file.

When P0EGIO = 0, all the pins of port 0E are set in the input mode. When an instruction that reads the data of the port register is executed at this time, the pin status is read.

When P0EGIO = 1, all the pins of port 0E are set in the output port, and the contents written to the output latch are output to the pins. When an instruction that reads the port status is executed with the port set in the output mode, the contents of the output latch, instead of the pin status, are read.

A pull-up resistor can be connected on-chip to this port through software. Whether the pull-up resistor is connected is specified by P0EGPU (bit 2 at address 0CH) of the register file. All the four-bit pins are pulled up when P0EGPU = 1. When P0EGPU = 0, the pull-up resistor is not connected.

P0EGIO is cleared to "0" at reset, and all the P0E pins are set in the input mode. The value of the output latch is also cleared to "0".

Table 11-6. Writing and Reading Port Register (0.6EH)

(n = 0 to 3)

P0EGIO RF: 2CH, bit 2	Input/Output Mode of Pin	BANK0 6EH	
		Write	Read
0	Input	Enabled Write to P0E latch	P0E pin status
1	Output		P0E latch contents

11.6 Port 0F ($P0F_0/\overline{\text{RLS}}$, $P0F_1/V_{REF}$)

Port 0F is a 2-bit input port and mapped at address 6FH of BANK0 of the data memory. A pull-up resistor can be connected on-chip bitwise to this port by mask option.

If a read instruction that reads the port register is executed when both pins of port 0F are used as input port pins, the higher 2 bits of the register are fixed to 0, and the pin statuses are read to the lower 2 bits. Executing a write instruction is meaningless as the contents of the port register remain unchanged.

The $P0F_0/\overline{\text{RLS}}$ pin is also used to input a standby mode release signal.

The $P0F_1/V_{REF}$ pin inputs a reference voltage to the A/D converter when even one of the bits of P0CnIDI (RF: address 1BH, n = 0 to 3) is set to "1". If an instruction is executed to read the port register when the $P0F_1/V_{REF}$ pin functions as the V_{REF} pin, bit 1 of address 6FH is always cleared to 0.

12. 8-BIT TIMERS/COUNTERS (TM0, TM1)

The μPD17149(A1) is provided with two 8-bit timers/counters: timer 0 (TM0) and timer 1 (TM1).

By using the count-up signal of timer 0 as the count pulse to timer 1, the two 8-bit timers can be used as a 16-bit timer.

Each timer is controlled through hardware manipulation by using the PUT or GET instruction or manipulation of the registers on the register file by using the PEEK or POKE instruction.

12.1 Configuration of 8-Bit Timers/Counters

Figure 12-1 shows the configuration of the 8-bit timers/counters. An 8-bit timer/counter consists of an 8-bit count register, an 8-bit modulo register, a comparator that compares the value of the count register with that of the modulo register, and a selector that selects the count pulse.

Cautions 1. The modulo register is a write register.
2. The count register is a read register.

Figure 12-1. Configuration of 8-Bit Timer/Counter

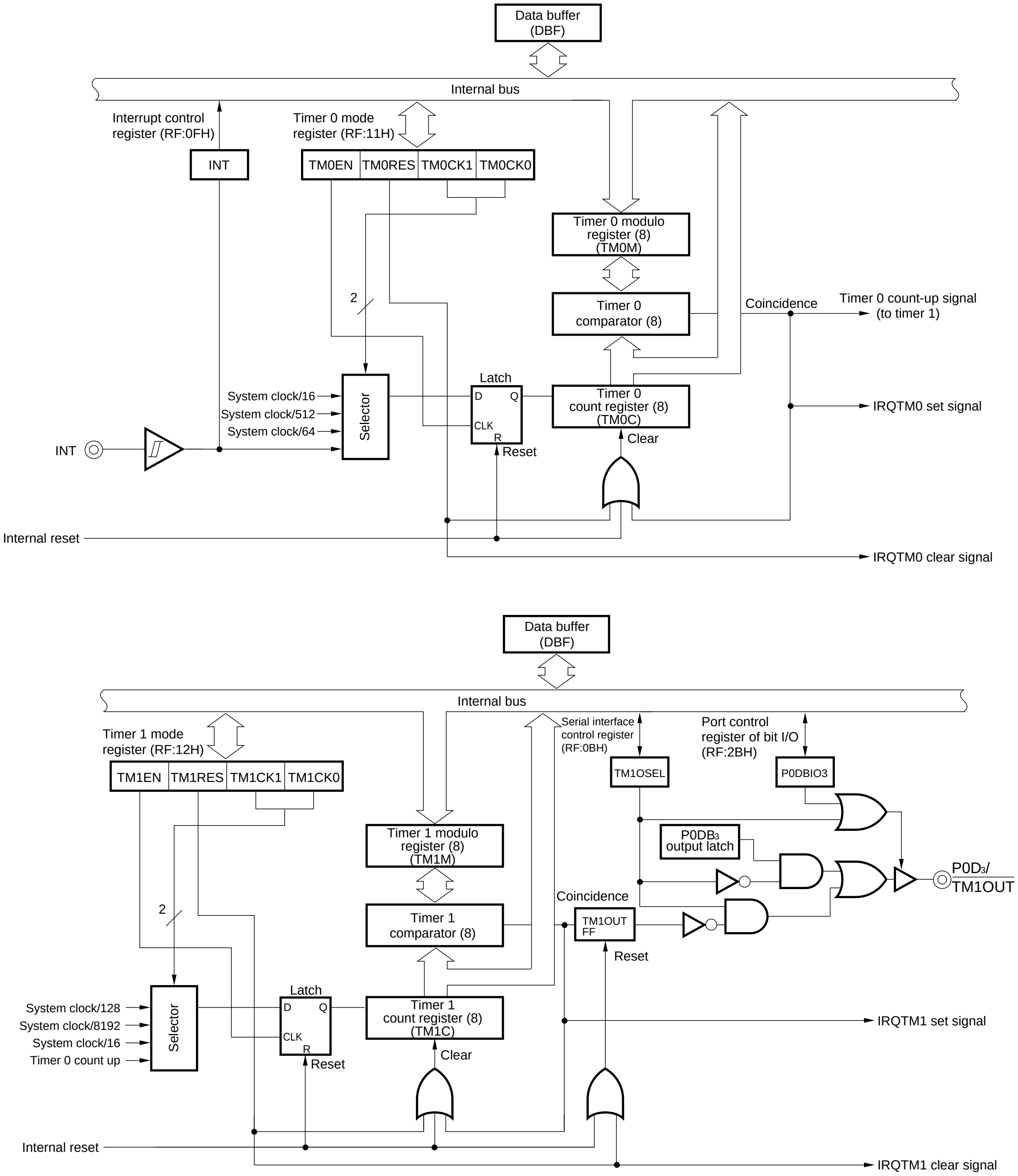


Figure 12-2. Timer 0 Mode Register

RF : 11H	Bit 3	Bit 2	Bit 1	Bit 0
	TM0EN	TM0RES	TM0CK1	TM0CK0
Read/write	R/W			
Initial value at reset	0	0	0	0

Read = R, write = W

TM0CK1	TM0CK0	Selects count pulse of timer 0
0	0	System clock/16
0	1	System clock/512
1	0	System clock/64
1	1	INT pin

TM0RES	Resets timer 0
0	Does not affect timer 0
1	Resets timer 0 count register and IRQTM0

Remark TM0RES is automatically cleared to 0 after it has been set to 1. When it is read, "0" is always read.

TM0EN	Timer 0 start command
0	Stops counting of timer 0
1	Resumes counting of timer 0

Remark TM0EN can be used as a status flag that detects the count status of timer 0 (1 : counting in progress, 0 : counting stopped)

Figure 12-3. Timer 1 Mode Register

RF : 12H	Bit 3	Bit 2	Bit 1	Bit 0
	TM1EN	TM1RES	TM1CK1	TM1CK0
Read/write	R/W			
Initial value at reset	1	0	0	0

TM1CK1	TM1CK0	Selects count pulse of timer 1
0	0	System clock/128
0	1	System clock/8192
1	0	System clock/16
1	1	Count-up signal from timer 0

TM1RES	Resets timer 1
0	Does not affect timer 1
1	Resets timer 1 count register and IRQTM1

Remark TM1RES is automatically cleared to 0 after it has been set to 1. When it is read, "0" is always read.

TM1EN	Timer 1 start command
0	Stops counting of timer 1
1	Resumes counting of timer 1

Remark TM1EN can be used as a status flag that detects the count status of timer 1 (1 : counting in progress, 0 : counting stopped)

13. BASIC INTERVAL TIMER (BTM)

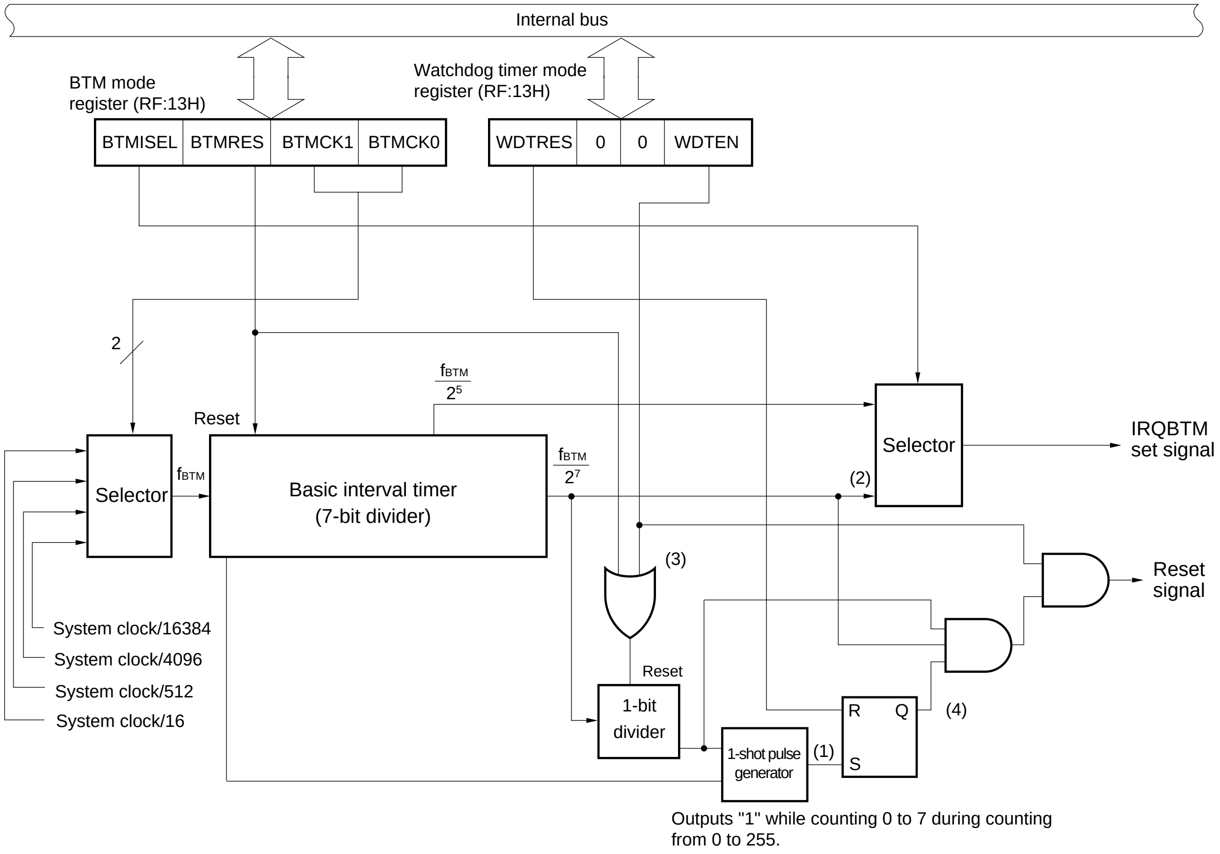
The μPD17149(A1) is provided with a 7-bit basic interval timer. This timer has the following functions:

(1) Generates reference time.
(2) Selects and counts wait time when standby mode is released.
(3) Watchdog timer function to detect program runaway.

13.1 Configuration of Basic Interval Timer

Figure 13-1 shows the configuration of the basic interval timer.

Figure 13-1. Configuration of Basic Interval Timer



Remark (1) to (4) in the figure correspond to the signals in the timing chart in Figure 13-4.

13.2 Registers Controlling Basic Interval Timer

The basic interval timer is controlled by the BTM mode register and watchdog timer mode register. Figures 13-2 and 13-3 show the configuration of each register.

Figure 13-2. BTM Mode Register

RF : 13H

	Bit 3	Bit 2	Bit 1	Bit 0
	BTMISEL	BTMRES	BTMCK1	BTMCK0
Read/write	R/W			
Initial value at reset	0	0	0	0

Read = R, Write = W

BTMCK1	BTMCK0	Selects count pulse to BTM
0	0	System clock/16 (1 instruction execution time)
0	1	System clock/16384 (1024 instruction execution time)
1	0	System clock/4096 (256 instruction execution time)
1	1	System clock/512 (32 instruction execution time)

BTMRES	Resets BTM
0	Does not affect basic interval timer (BTM)
1	Resets binary counter of basic interval timer (BTM)

Remark BTMRES is automatically cleared to 0 after it has been set to 1. When it is read, "0" is always read.

BTMISEL	Selects interval timer
0	Sets interval timer to 1/128 of count pulse
1	Sets interval timer to 1/32 of count pulse

Figure 13-3. Watchdog Timer Mode Register

RF : 03H

	Bit 3	Bit 2	Bit 1	Bit 0
	WDTRES	0	0	WDTEN
Read/write	R/W			
Initial value at reset	0	0	0	0

Read = R, Write = W

WDTEN	Enable watchdog timer
0	Stops watchdog timer.
1	Starts watchdog timer.

Remark 1. WDTEN cannot be cleared to 0 by program.

2. WDTEN is automatically cleared to 0 after it has been set to 1. When it is read, "0" is always read.

WDTRES	Resets watchdog timer
0	Does not affect watchdog timer.
1	Resets flip-flop that retains overflow carry of BTM used for watchdog timer.

Remark WDTRES is automatically cleared to 0 after it has been set to 1. When it is read, "0" is always read.

13.3 Watchdog Timer Function

The basic interval timer can also be used as a watchdog timer that detects a program runaway.

13.3.1 Function of watchdog timer

The watchdog timer is a counter that generates a reset signal at fixed time intervals. By inhibiting generation of this reset signal by program, the system can be reset (started from address 0000H) if the system becomes runaway due to external noise (if the watchdog timer is not reset within specific time).

This function allows the program to escape from the runaway status because a reset signal is generated at fixed time intervals even when the program jumps to an unexpected routine and enters an indefinite loop due to external noise.

13.3.2 Operation of watchdog timer

When WDTEN is set to 1, the 1-bit divider is enabled to operate, and the basic interval timer starts operating as an 8-bit watchdog timer.

Once the watchdog timer has been started, it cannot be stopped until the device is reset and WDTEN is cleared to 0.

Reset effected by the watchdog timer can be inhibited in the following two ways:

(1) Repeatedly set WDTRES in the program.

(2) Repeatedly set BTMRES in the program.

In the case of (1), WDTRES must be set while the count value of the watchdog timer is 8 to 191 (before it reaches 192). Therefore, program so that “SET1 WDTRES” is executed at least once in a cycle shorter than that in which the watchdog timer counts 184.

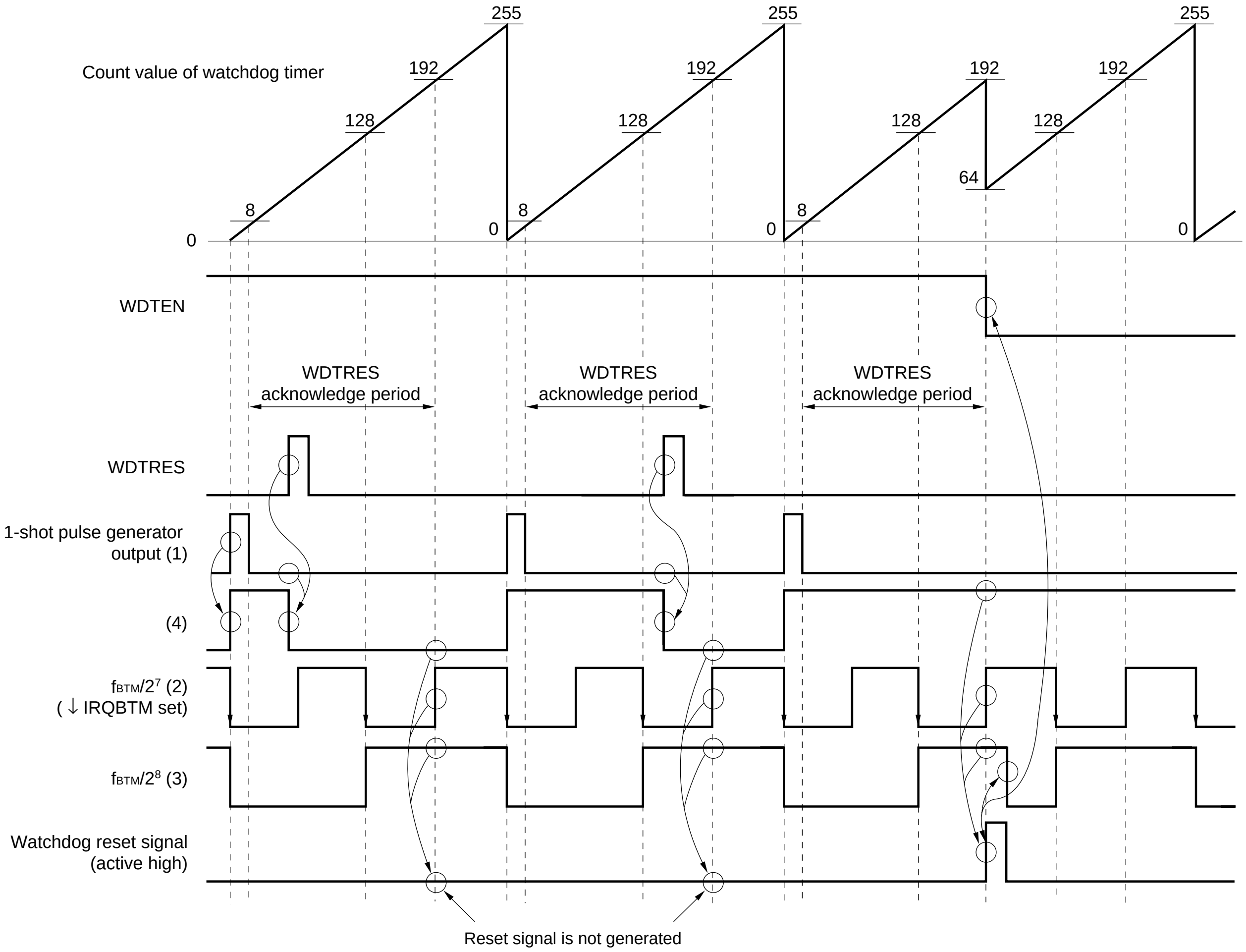
In the case of (2), BTMRES must be set before the basic interval timer (BTM) counts 128. Therefore, program so that “SET1 BTMRES” is executed at least once in a cycle shorter than that in which BTM counts 128. In this case, however, interrupts cannot be processed with BTM.

Caution BTM is not reset even if WDTEN is set. Therefore, before setting WDTEN first, be sure to set BTMRES to reset BTM.

Example

```
          ⋮
SET1 BTMRES
SET2 WDTEN, WDTRES
          ⋮
```

Figure 13-4. Timing Chart of Watchdog Timer (when WDTRES flag is used)


Count value of watchdog timer
255
255
255
192
192
192
192
128
128
128
128
64
8
8
8
0
0
0
0
WDTEN
WDTRES acknowledge period
WDTRES acknowledge period
WDTRES acknowledge period
WDTRES
1-shot pulse generator output (1)
(4)
fBTM/2^7 (2)
(↓ IRQBTM set)
fBTM/2^8 (3)
Watchdog reset signal (active high)
Reset signal is not generated

14. A/D CONVERTER

The μPD17149(A1) is provided with an A/D converter with 4 analog input channels ($P0C_0/ADC_0$-$P0C_3/ADC_3$) and a resolution of 8 bits.

This A/D converter is of the successive approximation type and operates in the following two modes:

① Successive mode in which 8-bit A/D conversion is sequentially performed starting from the most significant bit

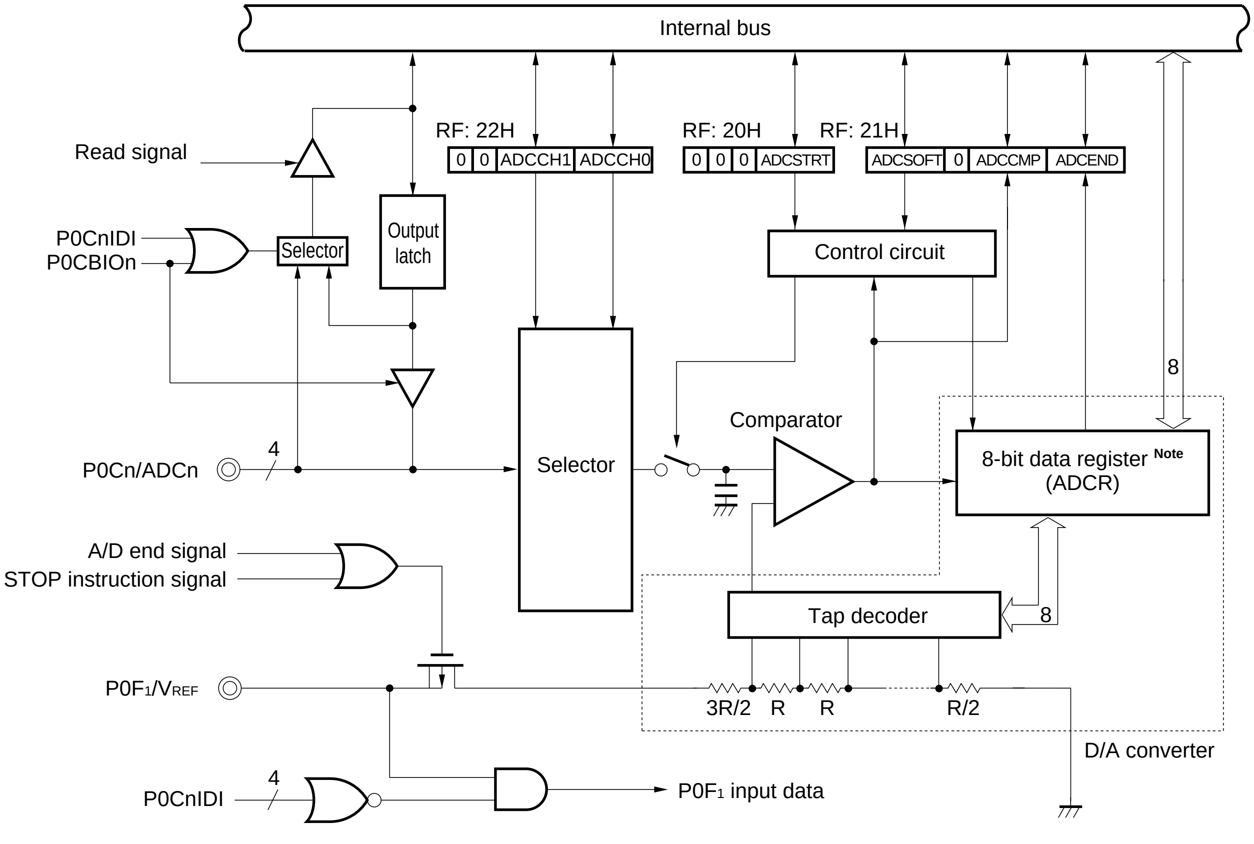
② Single mode in which an input analog voltage is compared with the set value of an 8-bit data register

14.1 Configuration of A/D Converter

Figure 14-1 shows the configuration of the A/D converter.

Figure 14-1. Block Diagram of A/D Converter

Remark n = 0 to 3



Note The 8-bit data register (ADCR) is cleared to 00H when the STOP instruction is executed.

14.2 Function of A/D Converter

(1) ADC$_0$ to ADC$_3$ pins

These pins input analog voltages to the four channels of the A/D converter. The analog voltages are converted into digital signals. The A/D converter is provided with a sample and hold circuit, and an analog input voltage being converted into a digital signal is internally held.

(2) V$_{REF}$ pin

This pin inputs a reference voltage to the A/D converter.

The signals input to ADC$_0$ to ADC$_3$ are converted into digital signals based on the voltage applied across V$_{REF}$ and GND. The A/D converter of the μPD17149(A1) has a function to automatically stop the current flowing into the V$_{REF}$ pin when the A/D converter does not operate. A current flows into the V$_{REF}$ pin in the following cases:

① **In successive mode (ADCSOFT = 0)**

Since the ADCSTRT flag has been set to 1 until the ADCEND flag is set to 1.

② **In single mode (ADCSOFT = 1)**

Since the ADCSTRT flag has been set to 1 or a value has been written to the 8-bit data register until the result of comparison by the comparator is written to the ADCCMP flag.

Remarks 1. If the HALT instruction is executed during A/D conversion, the A/D converter operates, in the successive mode, until the ADCEND flag is set, or in the single mode, until the result of conversion is stored to the ADCCMP flag. Therefore, a current flows to the V$_{REF}$ pin during this period.

2. A/D conversion in progress is stopped if the STOP instruction is executed. In this case, the A/D converter is initialized, and the current flowing to the V$_{REF}$ pin is cut (the A/D converter does not operate even if the STOP mode has been released).

(3) 8-bit data register (ADCR)

This is an 8-bit register that stores the result of A/D conversion of successive approximation type in the successive mode. The contents of this register are read by using the GET instruction. In the single mode, the contents of the 8-bit data register are converted into an analog voltage by an internal D/A converter and is compared by the comparator with an analog signal input from the ADCn pin. A value can be written to this register by using the PUT instruction.

(4) Comparator

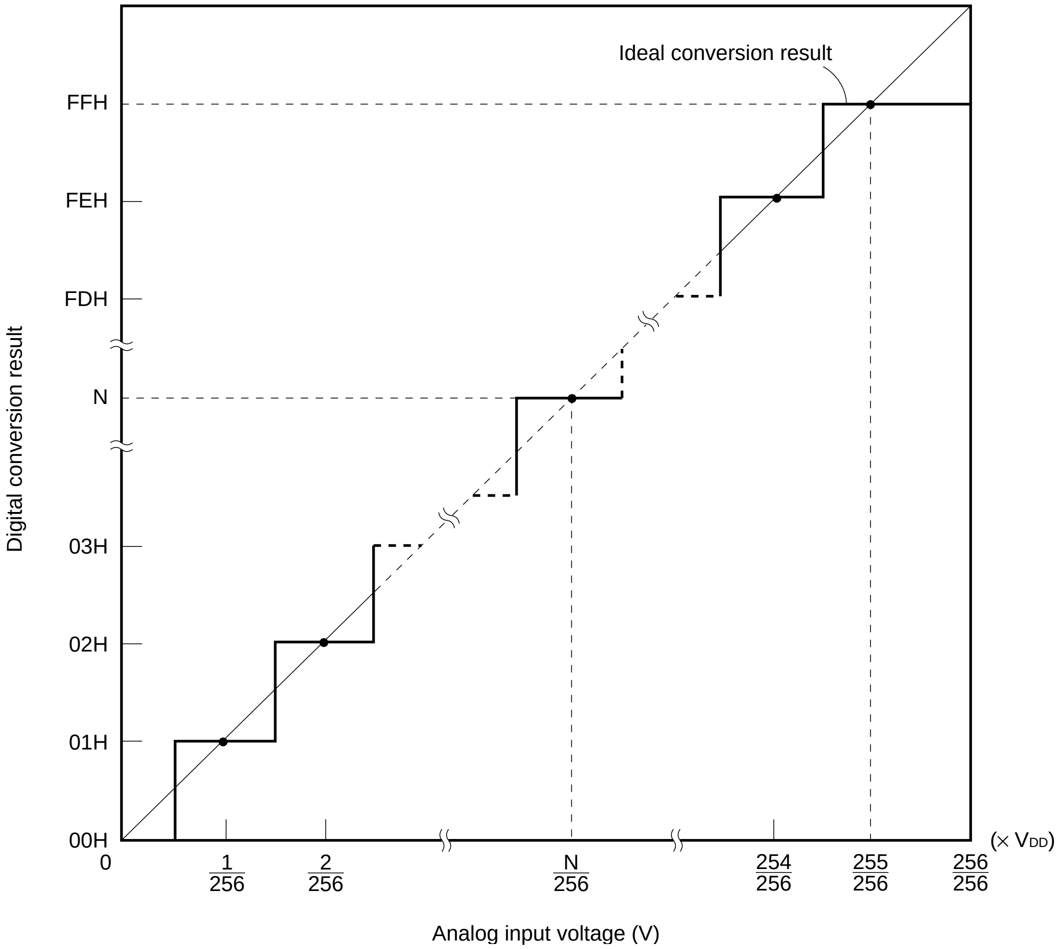
The comparator compares the analog input voltage with the voltage output by the D/A converter. If the analog input voltage is high, it outputs “1”; if the voltage is low, the comparator outputs “0”. The result of comparison is stored to the 8-bit data register (ADCR) in the successive mode, and to the ADCCMP flag in the single mode.

14.3 Operation of A/D Converter

The operation of the A/D converter can be executed in two modes, depending on the setting of the ADCSOFT flag: successive and single modes.

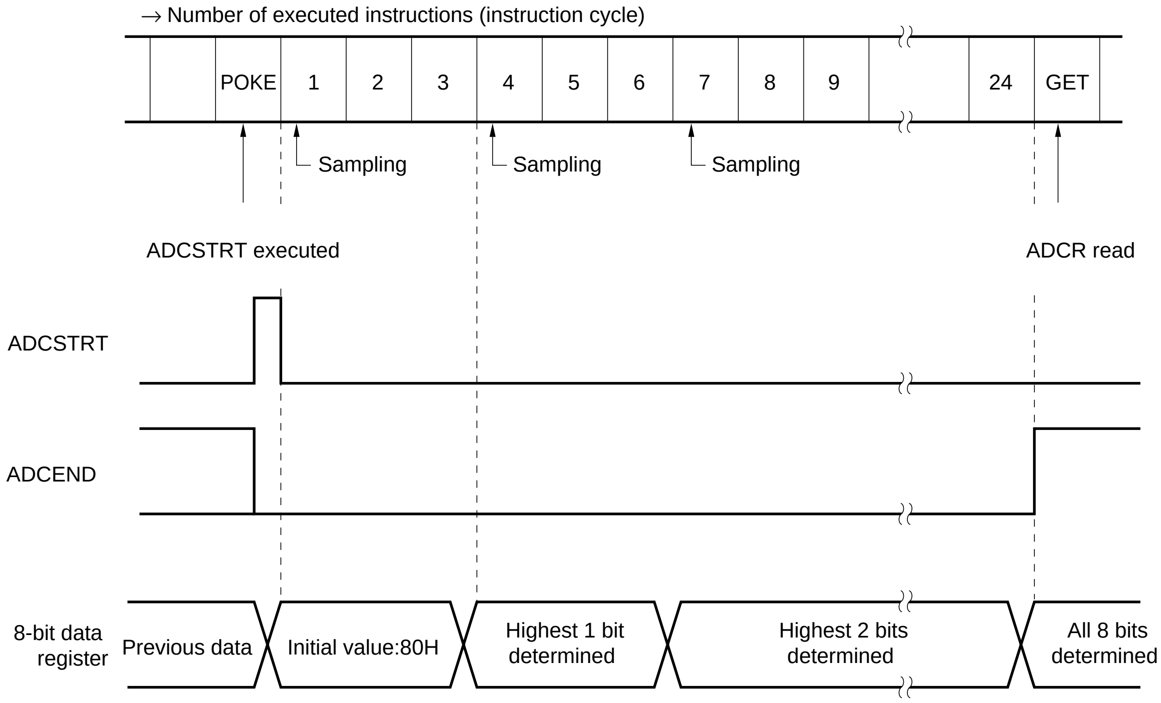
ADCSOFT	Operation Mode of A/D Converter
0	Successive mode (A/D conversion)
1	Single mode (compare operation)

Figure 14-2. Relationships between Analog Input Voltage and Digital Conversion Result



(1) Timing in successive mode (A/D conversion)

Figure 14-3. Timing in Successive Mode (A/D Conversion)

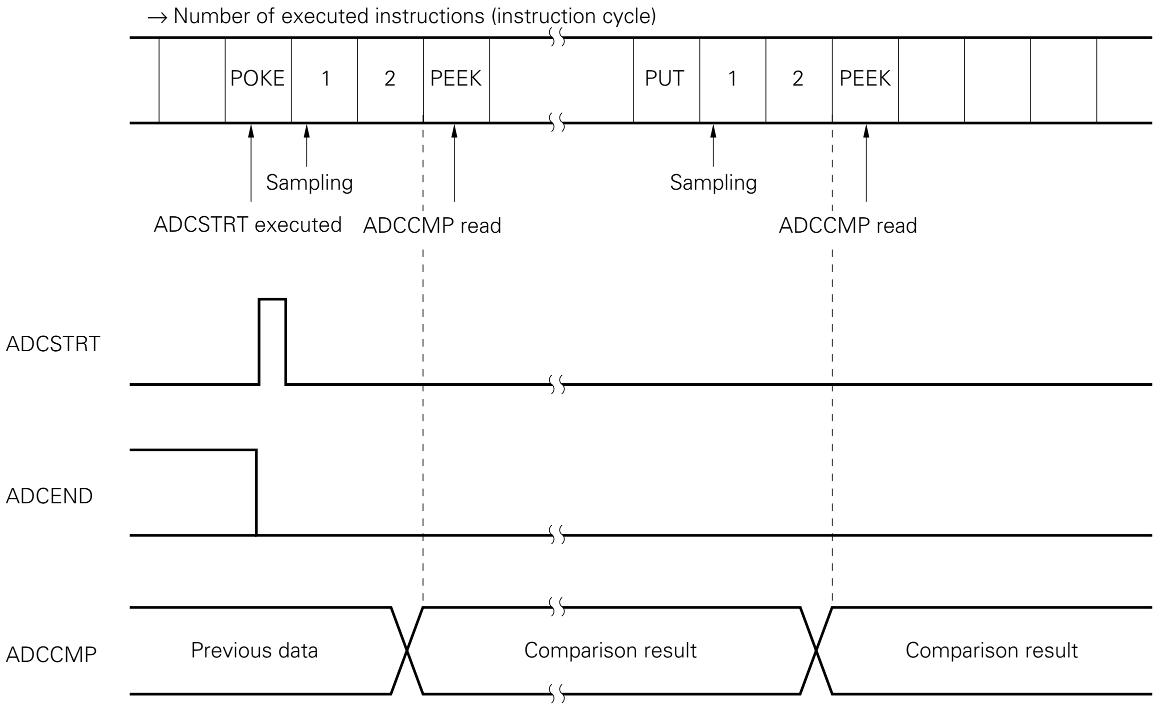


Caution **Sampling is performed eight times while A/D conversion is executed once. If the analog input voltage changes heavily during A/D conversion, A/D conversion cannot be performed accurately. To obtain an accurate conversion result, it is necessary to minimize the changes in the analog input voltage during A/D conversion.**

Remark One sampling time = 14/f_x (1.75 μs, at 8 MHz)
Sampling repeat cycle = 48/f_x (6 μs, at 8 MHz)
Sampling capacitor capacitance = 100 pF (MAX.)

(2) Timing in single mode (compare operation)

Figure 14-4. Timing in Single Mode (Compare Operation)



After 1 has been written to ADCSTRT in the single mode (execution of the POKE instruction), a value is stored to ADCCMP three instructions after, and the result of comparison can be read by the PEEK instruction. Even if data is set to ADCR (execution of the PUT instruction), comparison is started in the same manner as ADCSTRT, and the result of comparison can be read three instructions after.

The ADCCMP flag is cleared to 0 when reset is executed or when an instruction that writes data to ADCR is executed.

Caution **Be sure to set ADCSOFT to 1 before setting a value to ADCR. When ADCSOFT = 0, no value can be set to ADCR (the PUT ADCR, DBF instruction is invalidated).**

Remark Sampling time = 14/f_x (1.75 μs, at 8 MHz)
Sampling capacitor capacitance = 100 pF (MAX.)

15. SERIAL INTERFACE (SIO)

The serial interface of the μPD17149(A1) consists of an 8-bit shift register (SIOSFR), a serial mode register, and a serial clock counter, and is used to input/output serial data.

15.1 Function of Serial Interface

The serial interface can transmit or receive 8-bit data in synchronization with the clock by using three wires: serial clock input ($\overline{\text{SCK}}$), serial data output (SO), and serial data input (SI) pins. This serial interface can connect various peripheral I/O devices in a mode compatible with the method employed for the μPD7500 series and 75X series.

(1) Serial clock

Four types of serial clocks, three internal and one external, can be selected. If an internal clock is selected as the serial clock, the selected clock is automatically output to the $\text{P0D}_0/\overline{\text{SCK}}$ pin.

Table 15-1. Serial Clocks

SIOCK1	SIOCK0	Selected Serial Clock
0	0	External clock from $\overline{\text{SCK}}$ pin
0	1	System clock/16
1	0	System clock/128
1	1	System clock/1024

(2) Transfer operation

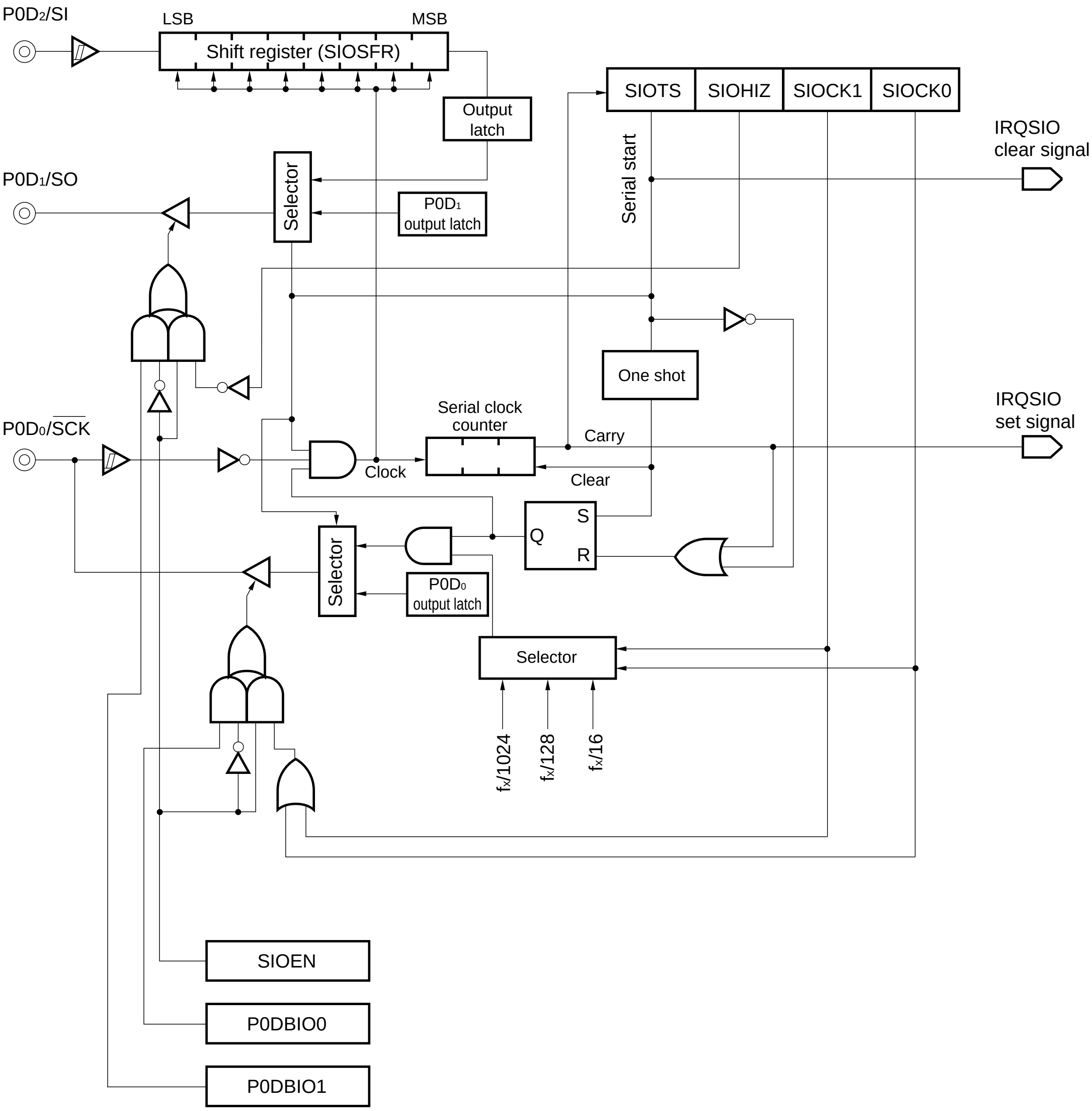
Each pin of port 0D ($\text{P0D}_0/\overline{\text{SCK}}$, P0D_1/SO, P0D_2/SI) functions as a serial interface pin when SIOEN is set to 1. If SIOTS is set to 1 at this time, the serial interface starts its operation in synchronization with the falling edge of the external or internal clock. If SIOTS is set, IRQSIO is automatically cleared.

Data is transferred starting from the most significant bit of the shift register in synchronization with the rising edge of the serial clock, and the information on the SI pin is stored to the shift register, starting from the least significant bit, in synchronization with the rising edge of the serial clock.

When 8-bit data has been completely transferred, SIOTS is automatically cleared, and IRQSIO is set.

Remark When serial transfer is executed, transfer is started only from the most significant bit of the contents of the shift register. In other words, transfer cannot be started from the least significant bit. The status of the SI pin is always loaded to the shift register in synchronization with the rising edge of the serial clock.

Figure 15-1. Block Diagram of Serial Interface



Caution **The output latch of the shift register is independent of the output latch of P0D1. Therefore, even if an output instruction is executed to P0D1, the status of the output latch of the shift register is not affected. The output latch of the shift register is cleared to "0" by RESET input. After that, it holds the status of the LSB of the previously transferred data.**

15.2 Operation Mode of 3-Wire Serial Interface

The serial interface can operate in the following two modes. When the serial interface function is selected, the P0D$_2$/SI pin always inputs data in synchronization with the serial clock.

- 8-bit transmission/reception mode (simultaneous transmission/reception)
- 8-bit reception mode (SO pin: high-impedance state)

Table 15-2. Operation Modes of Serial Interface

SIOEN	SIOHIZ	P0D$_0$/SI Pin	P0D$_1$/SO Pin	Operation Mode of Serial Interface
1	0	SI	SO	8-bit transmission/reception mode
1	1	SI	P0D$_1$ (input)	8-bit reception mode
0	×	P0D$_0$ (I/O)	P0D$_1$ (I/O)	General-purpose port mode

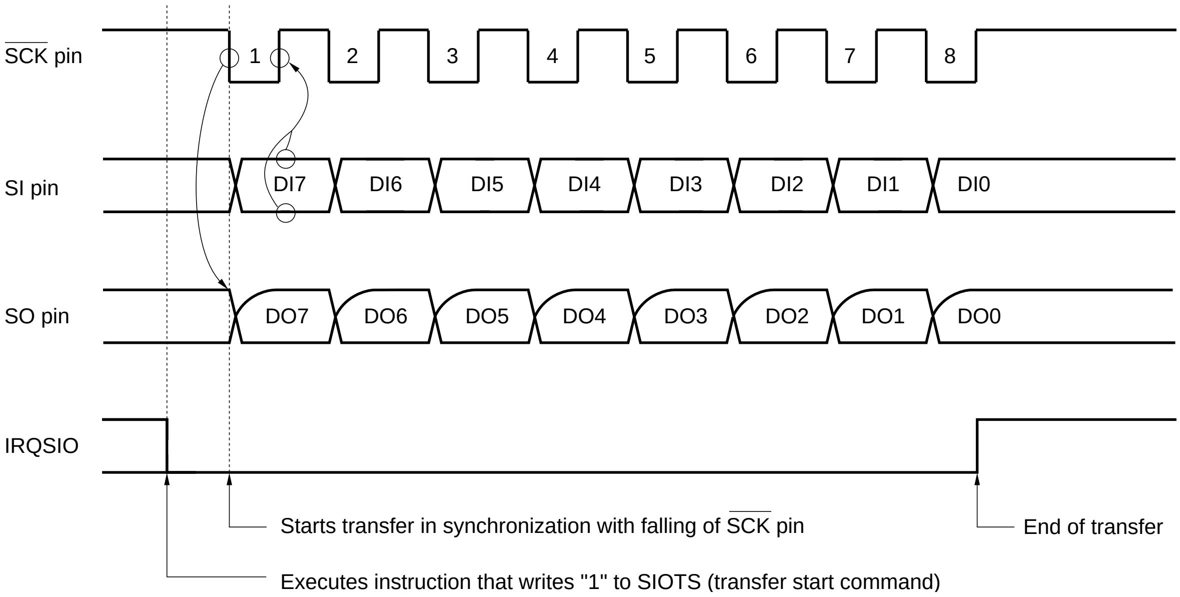
× : Don't care

(1) 8-bit transmission/reception mode (simultaneous transmission/reception)

Input or output of serial data is controlled by the serial clock. The MSB of the shift register is output to the SO line at the falling edge of the serial clock (SCK pin signal). The contents of the shift register are shifted 1 bit at the rising edge of the serial clock. At the same time, the data on the SI line is loaded to the LSB of the shift register.

The serial clock counter (3-bit counter) sets an interrupt request flag (IRQSIO <- 1) each time it has counted eight serial clocks.

Figure 15-2. Timing in 8-Bit Transmission/Reception Mode (Simultaneous Transmission/Reception)


$\overline{SCK}$ pin
1
2
3
4
5
6
7
8
SI pin
DI7
DI6
DI5
DI4
DI3
DI2
DI1
DI0
SO pin
DO7
DO6
DO5
DO4
DO3
DO2
DO1
DO0
IRQSIO
Starts transfer in synchronization with falling of $\overline{SCK}$ pin
End of transfer
Executes instruction that writes "1" to SIOTS (transfer start command)

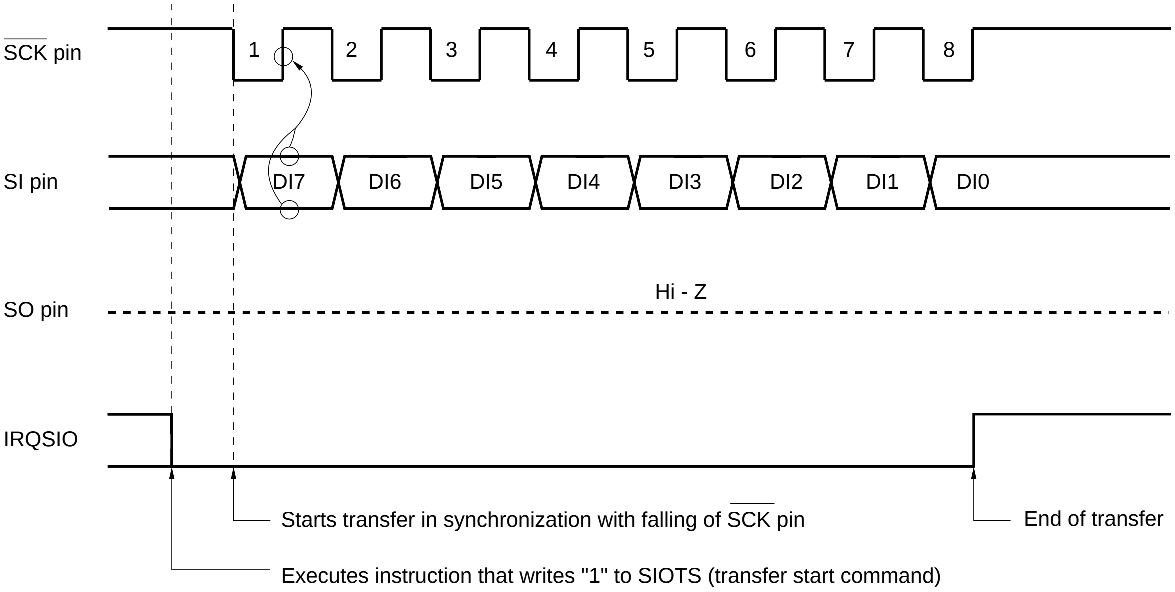
Remark DI: serial data input
DO: serial data output

(2) 8-bit reception mode (SO pin: high-impedance state)

The P0D1/SO pin goes into a high-impedance state when SIOHIZ = 1. If supply of the serial clock is started at this time by writing “1” to SIOTS, the serial interface only receives data.

Because the P0D1/SO pin goes into a high-impedance state, it can be used as an input port pin (P0D1).

Figure 15-3. Timing in 8-Bit Reception Mode


SCK pin
1
2
3
4
5
6
7
8
SI pin
DI7
DI6
DI5
DI4
DI3
DI2
DI1
DI0
SO pin
Hi - Z
IRQSIO
Starts transfer in synchronization with falling of SCK pin
End of transfer
Executes instruction that writes "1" to SIOTS (transfer start command)

Remark DI: serial data input

(3) Operation stop mode

When the value of SIOTS (RF: address 02H, bit 3) is 0, the serial interface is set in the operation stop mode. In this mode, serial transfer is not executed.

Because the shift register does not perform the shift operation in this mode, it can be used as an ordinary 8-bit register.

16. INTERRUPT FUNCTION

The μPD17149(A1) has five interrupt causes, of which four are internal and one is external, enabling various applications.

The interrupt control circuit of the μPD17149(A1) has the following features and can perform interrupt processing at extremely high speeds:

(a) Acknowledging an interrupt can be controlled by interrupt mask enable flag (INTE) and interrupt enable flag (IP×××).

(b) Interrupt request flags (IRQ×××) can be tested and cleared (occurrence of an interrupt can be checked by software).

(c) Multiple interrupts of up to 3 levels can be processed.

(d) The standby mode (STOP or HALT) can be released by an interrupt request (releasing condition can be selected by the interrupt enable flag).

Caution Only the BCD, CMP, CY, Z, and IXE flags are automatically saved to the stack by hardware when interrupt processing is performed. Up to three levels of multiple interrupts can be processed. If the peripheral hardware (timers, A/D converter, etc.) is accessed during interrupt processing, the contents of DBF and WR are not saved by the hardware. It is therefore recommended that DBF and WR be saved to the RAM by software at the beginning of interrupt processing, and that their contents be restored immediately before the interrupt processing.

16.1 Types of Interrupt Causes and Vector Addresses

All the interrupts of the μPD17149 (A1) are vectored interrupts, and therefore, program execution branches to a vector address corresponding to the interrupt cause when an interrupt has been acknowledged. Table 16-1 shows the types of interrupt causes and vector addresses.

If two or more interrupts occur at the same time, or if two or more pending interrupts are enabled all at once, processing is performed according to the priority shown in Table 16-1.

Table 16-1. Types of Interrupt Causes

Interrupt Cause	Priority	Vector Address	IRQ Flag	IP Flag	IEG Flag	Internal /External	Remark
INT pin (RF: 0FH, bit 0)	1	0005H	IRQ RF: 3FH, bit 0	IP RF: 2FH, bit 0	IEGMD0, 1 RF:1FH	External	Rising, falling, or both rising and falling edges selectable
Timer 0	2	0004H	IRQTM0 RF: 3EH, bit 0	IPTM0 RF: 2FH, bit 1	—	Internal	
Timer 1	3	0003H	IRQTM1 RF: 3DH, bit 0	IPTM1 RF: 2FH, bit 2	—	Internal	
Basic interval timer	4	0002H	IRQBTM RF: 3CH, bit 0	IPBTM RF: 2FH, bit 3	—	Internal	
Serial interface	5	0001H	IRQSIO RF: 3BH, bit 0	IPSIO RF: 2EH, bit 0	—	Internal	

16.2 Hardware of Interrupt Control Circuit

This section describes each flag of the interrupt control circuit.

(1) Interrupt request flags and interrupt enable flags

An interrupt request flag (IRQ×××) is set to 1 when an interrupt request is generated, and automatically cleared to 0 when interrupt processing is executed.

An interrupt enable flag (IP×××) is provided for each interrupt request flag. The corresponding interrupt is enabled when this flag is “1”, and disabled when the flag is “0”.

(2) EI/DI instruction

Whether an interrupt that has been acknowledged is executed is specified by the EI or DI instruction.

When the EI instruction is executed, an interrupt enable flag (INTE) that enables acknowledging an interrupt is set to 1. The INTE flag is not registered on the register file. Therefore, the status of this flag cannot be checked by an instruction.

The DI instruction clears the INTE flag to “0”, disabling all the interrupts.

The INTE flag is also cleared to 0 at reset, and therefore all the interrupts are disabled.

Table 16-2. Interrupt Request Flags and Interrupt Enable Flags

Interrupt Request Flag	Interrupt Request Flag Setting Signal	Interrupt Enable Flag
IRQ	Sets when edge of INT pin input signal is detected. Edge to be detected is selected by IEGMD0 and IEGMD1 flags.	IP
IRQTM0	Set by coincidence signal from timer 0.	IPTM0
IRQTM1	Set by coincidence signal from timer 1.	IPTM1
IRQBTM	Set by overflow from basic interval timer (reference time interval signal).	IPBTM
IRQSIO	Set when serial interface completes serial data transfer.	IPSIO

17. STANDBY FUNCTION

17.1 Outline of Standby Function

The current dissipation of the μPD17149(A1) can be reduced by using the standby function. This function can be effected in two modes: STOP and HALT.

The STOP mode stops the system clock. In this mode, the current dissipation by the CPU is minimized with only leakage current flowing. The CPU therefore does not operate, but the contents of the data memory are retained.

In the HALT mode, oscillation of the clock continues. However, supply of the clock to the CPU is stopped. Therefore, the CPU stops operating. This mode cannot reduce the current dissipation as much as the STOP mode. However, because the system clock continues oscillating, the operation can be started immediately after the HALT mode has been released. In both the STOP and HALT modes, the statuses of the data memory, registers, and the output latches of the output ports immediately before the standby mode is set are retained (except STOP 0000B). Therefore, set the port status so that the current dissipation of the entire system is reduced before the standby mode is set.

Table 17-1. Status in Standby Mode

		STOP Mode	HALT Mode
Setting instruction		STOP instruction	HALT instruction
Clock oscillation circuit		Stops oscillation	Continues oscillation
Operating status	CPU	• Stops operation	
	RAM	• Retains previous status	
	Port	• Retains previous status[Note]	
	TM0	• Can operate only when INT input is selected as count clock • Stops when system clock is selected (count value is retained)	• Operable
	TM1	• Stops operation (count value is reset to “0”) (count up is disabled)	• Operable
	BTM	• Stops operation (count value is retained)	• Operable
	SIO	• Can operate only when external clock is selected as serial clock[Note]	• Operable
	A/D	• Stops operation[Note] (ADCR <- 00H)	• Operable
	INT	• Can operate	• Operable

Note As soon as the STOP 0000B instruction is executed, the pins of these peripherals are set in the input port mode, even when the control signal functions of the pins are used.

Cautions 1. Be sure to execute the NOP instruction immediately before the STOP and HALT instructions.

2. If both the interrupt request flag and interrupt enable flag corresponding to an interrupt are set, and if the interrupt is specified to release the standby mode, the standby mode is not set even if the STOP or HALT instruction is executed.

17.2 HALT Mode

17.2.1 Setting HALT mode

The HALT mode is set when the HALT instruction is executed.

The operand of the HALT instruction, $b_3b_2b_1b_0$, specifies the condition under which the HALT mode is released.

Table 17-2. HALT Mode Releasing Condition

Format: HALT $b_3b_2b_1b_0$B

Bit	HALT mode releasing condition[Note 1]
b_3	Enables releasing HALT mode by IRQ××× when 1[Notes 2, 4]
b_2	Fixed to “0”
b_1	Enables forced release of HALT mode by IRQTM1 when 1[Notes 3, 4]
b_0	Enables releasing HALT mode by $\overline{\text{RLS}}$ input when 1[Note 4]

Notes 1. Only reset ($\overline{\text{RESET}}$ input or POC) is valid when HALT 0000B is specified.

2. IP××× must be set to 1.

3. The HALT mode is released regardless of the status of IPTM1.

4. Even if the HALT instruction is executed with IRQ××× = 1 or $\overline{\text{RLS}}$ input being low, the HALT instruction is ignored (treated as an NOP instruction), and the HALT mode is not set.

17.2.2 Start address after HALT mode is released

The start address from which the program execution is started after the HALT mode has been released differs depending on the interrupt enable condition and the condition under which the HALT mode has been released.

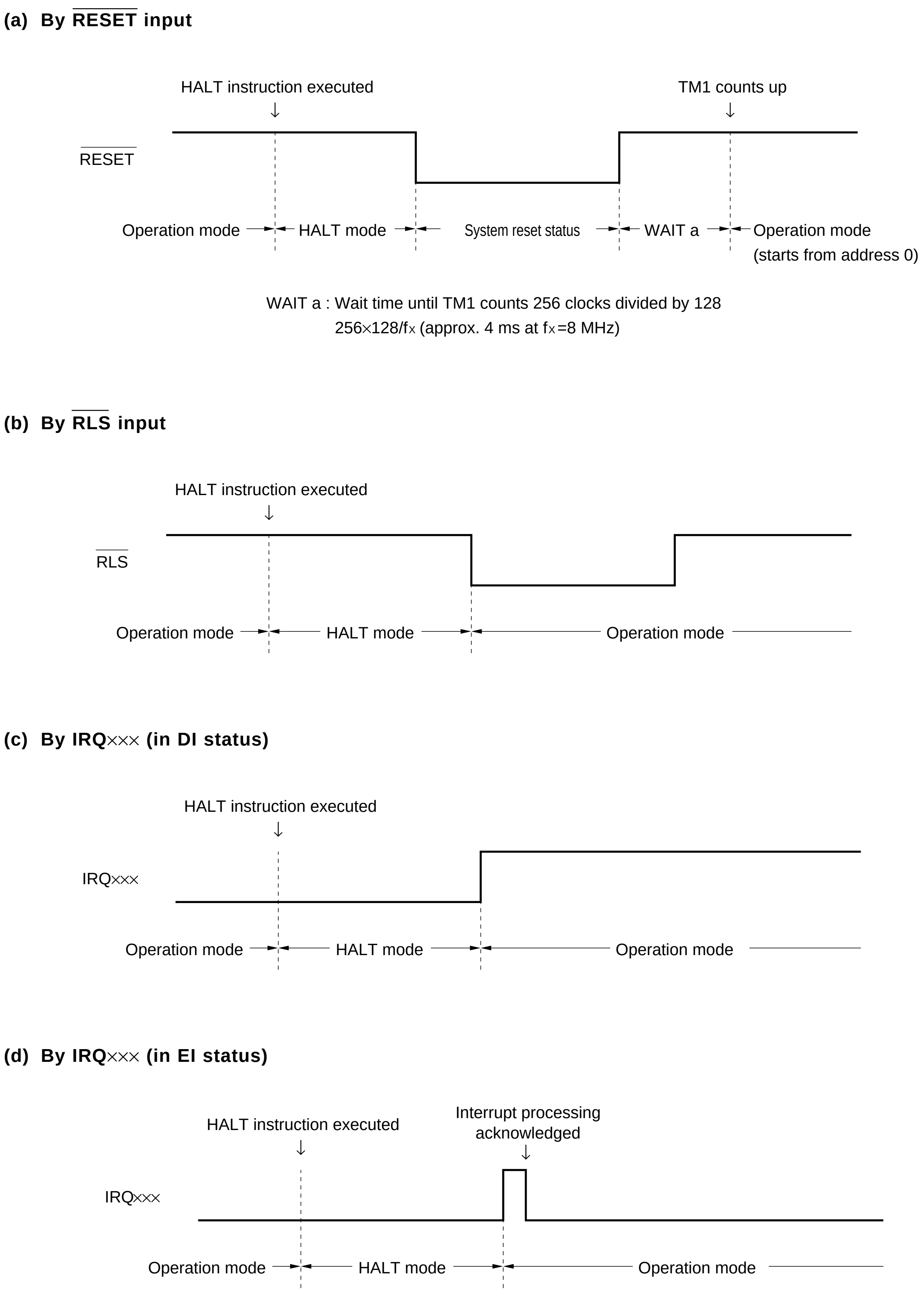
Table 17-3. Start Address after HALT Mode Is Released

Releasing Condition	Start Address after Release
Reset[Note 1]	Address 0
$\overline{\text{RLS}}$	Address next to that of HALT instruction
IRQ×××[Note 2]	Address next to that of HALT instruction in DI status
	Interrupt vector in EI status (if two or more IRQ××× flags are set, interrupt vector with higher priority)

Notes 1. $\overline{\text{RESET}}$ input and POC are valid as reset.

2. IP××× must be set to 1 except when the HALT mode is forcibly released by IRQTM1.

Figure 17-1. Releasing HALT Mode



(a) By $\overline{\text{RESET}}$ input

WAIT a : Wait time until TM1 counts 256 clocks divided by 128
256×128/f_X (approx. 4 ms at f_X=8 MHz)

(b) By $\overline{\text{RLS}}$ input

(c) By IRQ××× (in DI status)

(d) By IRQ××× (in EI status)

17.3 STOP Mode

17.3.1 Setting STOP mode

The STOP mode is set when the STOP instruction is executed.

The operand of the STOP instruction, $b_3b_2b_1b_0$, specifies the condition under which the STOP mode is released.

Table 17-4. STOP Mode Releasing Condition

Format: STOP $b_3b_2b_1b_0$B

Bit	STOP mode releasing condition[Note 1]
b_3	Enables releasing HALT mode by IRQ××× when 1[Notes 2, 4]
b_2	Fixed to “0”
b_1	Fixed to “0”
b_0	Enables releasing STOP mode by $\overline{\text{RLS}}$ input when 1[Notes 3, 4]

Notes 1. Only reset ($\overline{\text{RESET}}$ input or POC) is valid when STOP 0000B is specified. When STOP 0000B is executed, the internal circuitry of the microcontroller is initialized to the status immediately after reset.

2. IP××× must be set to 1. The STOP mode cannot be released by IRQTM1.

3. b_0 alone cannot be set to 1 (STOP 0001B is prohibited).
Before setting b_0 to 1, be sure to set b_3 to 1.

4. Even if the STOP instruction is executed with IRQ××× = 1 or the $\overline{\text{RLS}}$ input being low, the STOP instruction is ignored (treated as an NOP instruction), and the STOP mode is not set.

17.3.2 Start address after STOP mode is released

The start address from which the program execution is started after the STOP mode has been released differs depending on the condition under which the STOP mode has been released, and interrupt enable condition.

Table 17-5. Start Address after STOP Mode Is Released

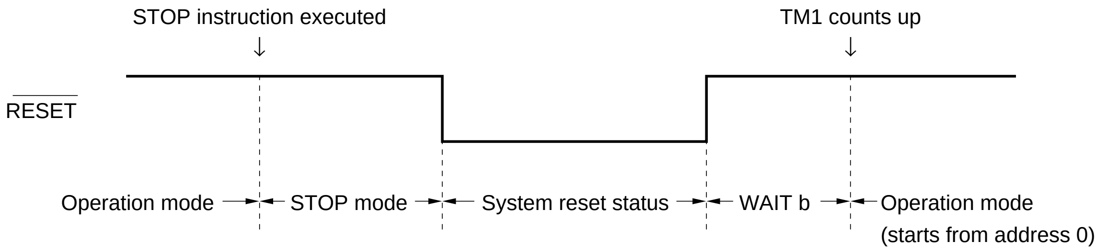
Releasing Condition	Start Address after Release
Reset[Note 1]	Address 0
$\overline{\text{RLS}}$	Address next to that of STOP instruction
IRQ×××[Note 2]	Address next to that of HALT instruction in DI status
	Interrupt vector in EI status (if two or more IRQ××× flags are set, interrupt vector with higher priority)

Notes 1. $\overline{\text{RESET}}$ input and POC are valid as reset.

2. IP××× must be set to 1. The STOP mode cannot be released by IRQTM1.

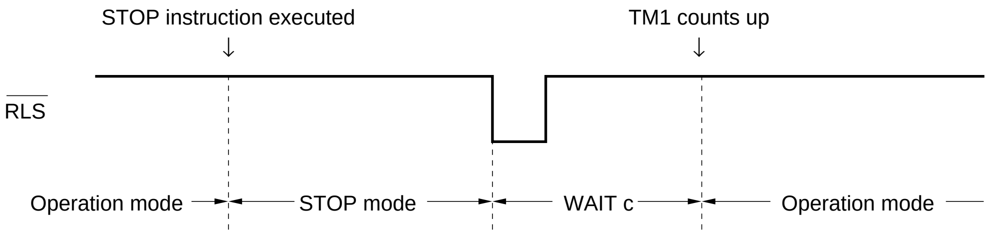
Figure 17-2. Releasing STOP Mode

(a) By $\overline{\text{RESET}}$ input



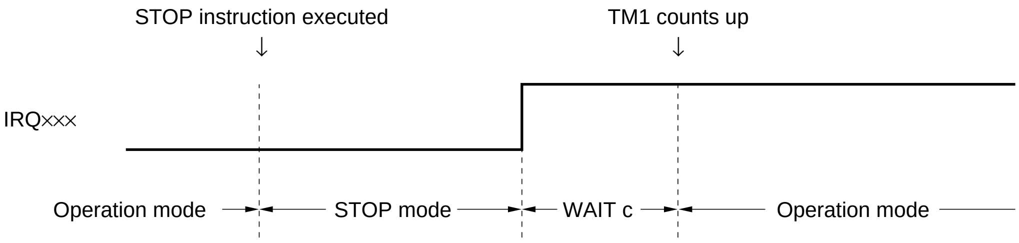
WAIT b : Wait time until TM1 counts 256 clocks divided by 128
$256 \times 128/f_X + \alpha$ (apporox. 4 ms + α at f_X = 8 MHz)
α : Oscillation growth time (differs depending on the oscillator)

(b) By $\overline{\text{RLS}}$ input



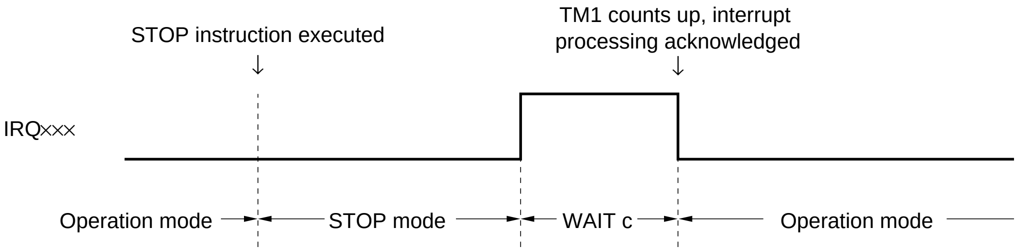
WAIT c : Wait time until TM1 counts clocks divided by m n times
$n \times m/f_X + \alpha$ (n and m are values immediately before STOP mode is set)
α : Oscillation growth time (differs depending on the oscillator)

(c) By IRQ××× (in DI status)



WAIT c : Wait time until TM1 counts clocks divided by m n times
$n \times m/f_X + \alpha$ (n and m are values immediately before STOP mode is set)
α : Oscillation growth time (differs depending on the oscillator)

(d) By IRQ××× (in EI status)


TM1 counts up, interrupt processing acknowledged
STOP instruction executed
IRQ×××
Operation mode
STOP mode
WAIT c
Operation mode

WAIT c : Wait time until TM1 counts clocks divided by m n times
$n \times m/f_X + \alpha$ (n and m are values immediately before STOP mode is set)
α : Oscillation growth time (differs depending on the oscillator)

18. RESET

The μPD17149 (A1) can be reset not only by the $\overline{\text{RESET}}$ input, but also by the internal POC circuit that detects a supply voltage drop, watchdog timer function that resets the microcontroller if program runaway occurs, and overflow or underflow of the address stack. Note, however, that the internal POC circuit is a mask option.

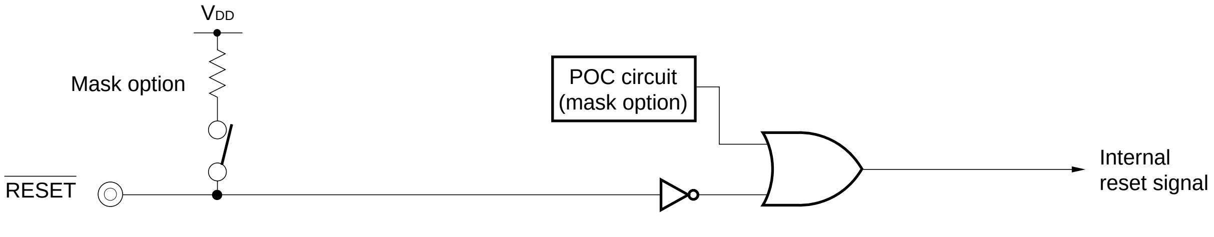
18.1 Reset Function

The reset function initializes the device operation. How the device is initialized differs depending on the type of reset.

Table 18-1. Hardware Status at Reset

Type of Reset Hardware		• $\overline{\text{RESET}}$ Input during Operation • Reset by Internal POC Circuit	• $\overline{\text{RESET}}$ Input in Standby Mode • Reset by Internal POC Circuit in Standby Mode	• Overflow of Watchdog Timer • Overflow and Underflow of Stack
Program counter		0000H	0000H	0000H
Port	Input/output	Input	Input	Input
	Contents of output latch	0	0	Undefined
General-purpose data memory	General-purpose data memory (except DBF)	Undefined	Retains contents	Undefined
	DBF	Undefined	Undefined	Undefined
	System register (except WR)	0	0	0
	WR	Undefined	Retains contents	Undefined
Control register		SP = 5H, IRQTM1 = 1, TM1EN = 1, IRQBTM = 1, INT = status at that time. Others are 0. Refer to 8. REGISTER FILE (RF).		SP = 5H, INT = status at that time. Others retain contents.
Timer 0 and timer 1	Count register	00H	00H	Timer 0: 00H, timer 1: undefined
	Modulo register	FFH	FFH	FFH
Binary counter of basic interval timer		Undefined	Undefined	Undefined. However, 40H if watchdog timer overflows.
Serial interface	Shift register (SIOSFR)	Undefined	Retains contents	Undefined
	Output latch	0	0	Undefined
Data register of A/D converter (ADCR)		00H	00H	00H

Figure 18-1. Configuration of Reset Block



18.2 Reset Operation

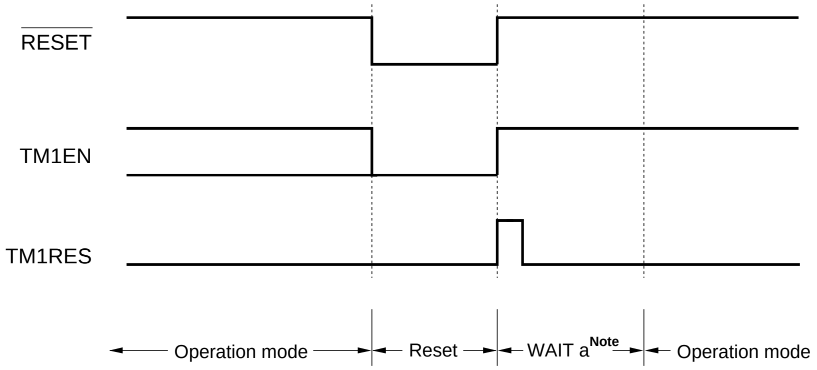
Figure 18-2 shows the operation when the system is reset by using the $\overline{\text{RESET}}$ pin.

When the $\overline{\text{RESET}}$ pin is made high, oscillation of the system clock is started, oscillation stabilization wait time specified by timer 1 elapses, and program execution is started from address 0000H.

These operations are also performed if the system is reset by the POC circuit.

If the system is reset by using an overflow of the watchdog timer or an overflow or underflow of the stack, the oscillation stabilization wait time (WAIT a) does not elapse, and program execution is started from address 0000H after the internal circuitry has been initialized.

Figure 18-2. Reset Operation



Note Oscillation stabilization wait time. An operation mode is set when system clock is counted 128 × 256 times by timer 1 (time required to executed 2048 instructions: approx. 4 ms at 8 MHz).

19. POC CIRCUIT (MASK OPTION)

The POC circuit monitors the supply voltage. When the supply voltage is turned ON/OFF, it automatically resets the internal circuitry of the microcontroller. This circuit can be used in an application circuit with a clock frequency of 400 kHz to 4 MHz.

The μPD17149 (A1) can be provided with the POC circuit by mask option.

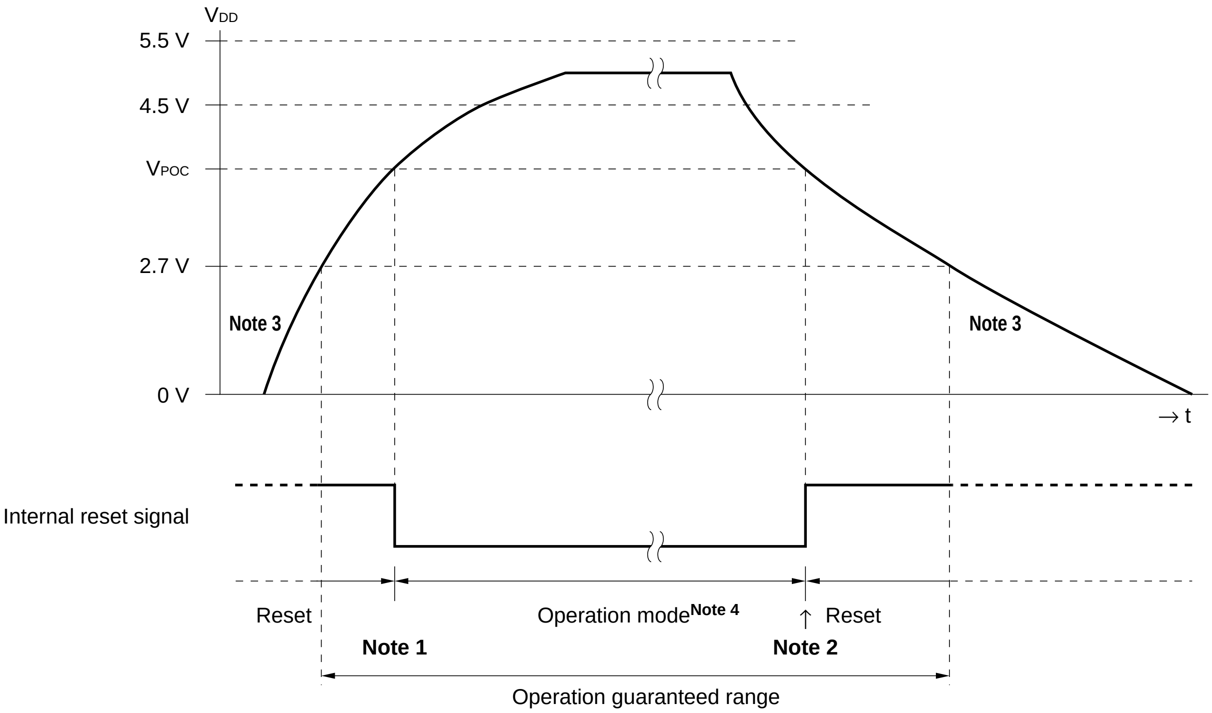
Caution The POC circuit is not provided to the PROM model (μPD17P149).

19.1 Function of POC Circuit

The POC circuit has the following functions:

- Generates internal reset signal when $V_{DD} \leq V_{POC}$
- Clears internal reset signal when $V_{DD} > V_{POC}$
  (where, V_{DD}: supply voltage, V_{POC}: POC detection voltage)

Figure 19-1. Operation of POC Circuit



Notes 1. Actually, oscillation stabilization wait time specified by timer 1 elapses before the operation mode is set. This time is equal to that required for executing about 2048 instructions (approx. 8 ms at 4 MHz).

2. To reset the microcontroller again when the supply voltage drops, the status in which the voltage drops below V_{POC} must be maintained at least for the duration of the reset detection pulse width t_{SAMP}.
Therefore, reset is actually effected with a delay time of up to t_{SAMP}.

3. The operation is not guaranteed if the supply voltage drops below the rated minimum value (2.7 V).
However, the POC circuit is designed to generate the internal reset signal so long as it is possible, regardless of oscillation. Therefore, the internal circuitry is reset when the voltage supplied to it has reached the level at which the circuitry can operate.

4. If the supply voltage abruptly increases (3 V/ms MIN.), the POC circuit may generate the internal reset signal, even in an operation mode, to prevent program runaway.

Remark For the values of V_{POC} and t_{SAMP}, refer to **22. ELECTRICAL SPECIFICATIONS**.

19.2 Conditions to Use POC Circuit

The POC circuit can be used when the application circuit satisfies the following conditions:

- The application circuit does not require a high reliability.
- The operating voltage must range from 4.5 to 5.5 V.
- The clock frequency must range from 400 kHz to 4 MHz.
- The supply voltage must satisfy the ratings of the POC circuit.

Cautions 1. If the application circuit requires an extremely high reliability, design the circuit so that the $\overline{\text{RESET}}$ signal is input from an external source.

2. The current dissipation in the standby mode slightly increases if the POC circuit is used.

Remark The guaranteed operating voltage range of the POC circuit is V_{DD} = 2.7 to 5.5 V.

20. INSTRUCTION SET

20.1 Outline of Instruction Set

b_{15} b_{14}-b_{11}		0		1	
BIN	HEX				
0000	0	ADD	r, m	ADD	m, #n4
0001	1	SUB	r, m	SUB	m, #n4
0010	2	ADDC	r, m	ADDC	m, #n4
0011	3	SUBC	r, m	SUBC	m, #n4
0100	4	AND	r, m	AND	m, #n4
0101	5	XOR	r, m	XOR	m, #n4
0110	6	OR	r, m	OR	m, #n4
0111	7	INC	AR		
		INC	IX		
		MOVT	DBF, @AR		
		BR	@AR		
		CALL	@AR		
		RET			
		RETSK			
		EI			
		DI			
		RETI			
		PUSH	AR		
		POP	AR		
		GET	DBF, p		
		PUT	p, DBF		
		PEEK	WR, rf		
		POKE	rf, WR		
		RORC	r		
		STOP	s		
		HALT	h		
		NOP			
1000	8	LD	r, m	ST	m, r
1001	9	SKE	m, #n4	SKGE	m, #n4
1010	A	MOV	@r, m	MOV	m, @r
1011	B	SKNE	m, #n4	SKLT	m, #n4
1100	C	BR	addr (page 0)	CALL	addr
1101	D	BR	addr (page 1)	MOV	m, #n4
1110	E			SKT	m, #n
1111	F			SKF	m, #n

20.2 Legend

AR	: address register
ASR	: address stack register indicated by stack pointer
addr	: program memory address (lower 11 bits)
BANK	: bank register
CMP	: compare flag
CY	: carry flag
DBF	: data buffer
h	: halt release condition
INTEF	: interrupt enable flag
INTR	: register automatically saved to the stack when interrupt processing is performed
INTSK	: interrupt stack register
IX	: index register
MP	: data memory row address pointer
MPE	: memory pointer enable flag
m	: data memory address indicated by m_R, m_C
m_R	: data memory row address (high)
m_C	: data memory column address (low)
n	: bit position (4 bits)
n4	: immediate data (4 bits)
PAGE	: page (bit 11 of program counter)
PC	: program counter
p	: peripheral address
p_H	: peripheral address (higher 3 bits)
p_L	: peripheral address (lower 4 bits)
r	: general register column address
rf	: register file address
rf_R	: register file row address (higher 3 bits)
rf_C	: register file column address (lower 4 bits)
SP	: stack pointer
s	: stop release condition
WR	: window register
(×)	: contents addressed by ×

20.3 Instruction Set

Instruction	Mnemonic	Operand	Operation	Instruction code			
				op code	Operand		
Addition	ADD	r, m	(r) ← (r) + (m)	00000	m_R	m_C	r
		m, #n4	(m) ← (m) + n4	10000	m_R	m_C	n4
	ADDC	r, m	(r) ← (r) + (m) + CY	00010	m_R	m_C	r
		m, #n4	(m) ← (m) + n4 + CY	10010	m_R	m_C	n4
	INC	AR	AR ← AR + 1	00111	000	1001	0000
		IX	IX ← IX + 1	00111	000	1000	0000
Subtraction	SUB	r, m	(r) ← (r) – (m)	00001	m_R	m_C	r
		m, #n4	(m) ← (m) – n4	10001	m_R	m_C	n4
	SUBC	r, m	(r) ← (r) – (m) – CY	00011	m_R	m_C	r
		m, #n4	(m) ← (m) – n4 – CY	10011	m_R	m_C	n4
Logical operation	OR	r, m	(r) ← (r) ∨ (m)	00110	m_R	m_C	r
		m, #n4	(m) ← (m) ∨ n4	10110	m_R	m_C	n4
	AND	r, m	(r) ← (r) ∧ (m)	00100	m_R	m_C	r
		m, #n4	(m) ← (m) ∧ n4	10100	m_R	m_C	n4
	XOR	r, m	(r) ← (r) ⊻ (m)	00101	m_R	m_C	r
		m, #n4	(m) ← (m) ⊻ n4	10101	m_R	m_C	n4
Judgment	SKT	m, #n	CMP ← 0, if (m) ∧ n = n, then skip	11110	m_R	m_C	n
	SKF	m, #n	CMP ← 0, if (m) ∧ n = 0, then skip	11111	m_R	m_C	n
Comparison	SKE	m, #n4	(m) – n4, skip if zero	01001	m_R	m_C	n4
	SKNE	m, #n4	(m) – n4, skip if not zero	01011	m_R	m_C	n4
	SKGE	m, #n4	(m) – n4, skip if not borrow	11001	m_R	m_C	n4
	SKLT	m, #n4	(m) – n4, skip if borrow	11011	m_R	m_C	n4
Rotation	RORC	r	→ CY → (r) b_3 → (r) b_2 → (r) b_1 → (r) b_0	00111	000	0111	r
Transfer	LD	r, m	(r) ← (m)	01000	m_R	m_C	r
	ST	m, r	(m) ← (r)	11000	m_R	m_C	r

	MOV	@r, m	if MPE = 1: (MP, (r)) ← (m)
			if MPE = 0: (BANK, m_R, (r)) ← (m)
				01010	m_R	m_C	r

		m, @r	if MPE = 1: (m) ← (MP, (r))
			if MPE = 0: (m) ← (BANK, m_R, (r))
				11010	m_R	m_C	r

		m, #n4	(m) ← n4	11101	m_R	m_C	n4
	MOVT	DVF, @AR	SP ← SP –1, ASR ← PC, PC ← AR, DBF ← (PC), PC ← ASR, SP ← SP +1	00111	000	0001	0000
	PUSH	AR	SP ← SP –1, ASR ← AR	00111	000	1101	0000
	POP	AR	AR ← ASR, SP ← SP +1	00111	000	1100	0000
	PEEK	WR, rf	WR ← (rf)	00111	rf_R	0011	rf_C
	POKE	rf, WR	(rf) ← WR	00111	rf_R	0010	rf_C
	GET	DBF, p	DBF ← (p)	00111	p_H	1011	p_L
	PUT	p, DBF	(p) ← DBF	00111	p_H	1010	p_L

Instruction	Mnemonic	Operand	Operation	Instruction code			
				op code	Operand		
Branch	BR	addr	**Note**	**Note**	addr		
		@AR	PC ← AR	00111	000	0100	0000
Subroutine	CALL	addr	SP ← SP – 1, ASR ← PC, PC ← addr	11100	addr		
		@AR	SP ← SP – 1, ASR ← PC, PC ← AR	00111	000	0101	0000
	RET		PC ← ASR, SP ← SP + 1	00111	000	1110	0000
	RETSK		PC ← ASR, SP ← SP + 1 and skip	00111	001	1110	0000
	RETI		PC ← ASR, INTR ← INTSK, SP ← SP + 1	00111	100	1110	0000
Interrupt	EI		INTEF ← 1	00111	000	1111	0000
	DI		INTEF ← 0	00111	001	1111	0000
Others	STOP	s	STOP	00111	010	1111	s
	HALT	h	HALT	00111	011	1111	h
	NOP		No operation	00111	100	1111	0000

Note The operation and op code of "BR addr" of the μPD17145(A1), 17147(A1), and μPD17149(A1) are as follows:

(a) μPD17145(A1), 17147(A1)

Mnemonic	Operand	Operation	op code
BR	addr	PC ← addr, PAGE ← 0	01100

(b) μPD17149(A1)

Mnemonic	Operand	Operation	op code
BR	addr	PC ← addr, PAGE ← 0	01100
		PC ← addr, PAGE ← 1	01101

20.4 Assembler (AS17K) Embedded Macro Instruction

Legend

flag n:	FLG type symbol
< >:	Can be omitted

	Mnemonic	Operand	Operation	n
Embedded macro	SKTn	flag 1, …flag n	if (flag 1) to (flag n) = all “1”, then skip	1 ≤ n ≤ 4
	SKFn	flag 1, …flag n	if (flag 1) to (flag n) = all“0”, then skip	1 ≤ n ≤ 4
	SETn	flag 1, …flag n	(flag 1) to (flag n) ← 1	1 ≤ n ≤ 4
	CLRn	flag 1, …flag n	(flag 1) to (flag n) ← 0	1 ≤ n ≤ 4

	NOTn	flag 1, …flag n	if (flag n) = “0”, then (flag n) ← 1
			if (flag n) = “1”, then (flag n) ← 0
				1 ≤ n ≤ 4

	INITFLG	<NOT> flag 1,
		…<<NOT> flag n>
			if description = NOT flag n, then (flag n) ← 0
			if description = flag n, then (flag n) ← 1
				1 ≤ n ≤ 4

	BANKn		(BANK) ← n	n = 0

21. ASSEMBLER RESERVED WORDS

21.1 Mask Option Directive

The μPD17149 (A1) has the following mask options:

- Internal pull-up resistor of $\overline{\text{RESET}}$ pin
- Internal pull-up resistor of $P0F_1$ and $P0F_0$ pins
- Internal pull-up resistor of INT pin
- Internal POC circuit

When developing a program, it is necessary to specify all the above mask options in the source program by using a mask option definition directive (pseudo instruction).

21.1.1 Specifying mask option

The mask option is described in the assembler source program by using the following directives:

- OPTION directive, ENDOP directive
- Mask option definition directive

(1) OPTION and ENDOP directives

These directives specify the range in which the mask option is specified (mask option definition block). Specify the mask option by describing a mask option definition directive in the area sandwiched between the OPTION and ENDOP directives.

Format

Symbol field	Mnemonic field	Operand field	Comment field
[label:]	OPTION		[;comment]
	⋮		
	ENDOP		

(2) Mask option definition directives

Table 21-1. Mask Option Definition Directives

Option	Definition Directive and Format	Operand	Defined Contents
Internal pull-up resistor of $\overline{\text{RESET}}$ pin	OPTRES <operand>	OPEN	None
		PULLUP	Defined
Internal pull-up resistor of $P0F_1$ and $P0F_0$ pins	OPTP0F <operand 1>, <operand 2>[Note]	OPEN	None
		PULLUP	Defined
Internal pull-up resistor of INT pin	OPTINT <operand>	OPEN	None
		PULLUP	Defined
Internal POC circuit	OPTPOC <operand>	NOUSE	Not used
		USE	Used

Note <operand 1> specifies the mask option of the $P0F_1$ pin, and <operand 2> specifies that of the $P0F_0$ pin.

(3) Example of mask option description

```
; Example of describing mask option of the μPD17149 (A1)

MASK_OPTION:

    OPTION                 ; start of mask option definition block
    OPTRES  PULLUP         ; connects internal pull-up resistor to RESET pin
    OPTP0F  PULLUP, OPEN   ; connects internal pull-up resistor to P0F1, and leaves P0F0 open (exter-
                             nally pulled up)
    OPTINT  PULLUP         ; connects internal pull-up resistor to INT pin
    OPTPOC  NOUSE          ; internal POC circuit is not used
    ENDOP                  ; End of mask option definition block
```

21.2 Reserved Symbols

The following tables show the reserved symbols defined by the device file (AS17149) of the μPD17149(A1):

System register (SYSREG)

Symbol Name	Attribute	Value	Read/Write	Description
AR3	MEM	0.74H	R	Bits b15-b12 of address register
AR2	MEM	0.75H	R/W	Bits b11-b8 of address register
AR1	MEM	0.76H	R/W	Bits b7-b4 of address register
AR0	MEM	0.77H	R/W	Bits b3-b0 of address register
WR	MEM	0.78H	R/W	Window register
BANK	MEM	0.79H	R/W	Bank register
IXH	MEM	0.7AH	R/W	Index register, high
MPH	MEM	0.7AH	R/W	Data memory row address pointer, high
MPE	FLG	0.7AH.3	R/W	Memory pointer enable flag
IXM	MEM	0.7BH	R/W	Index register, middle
MPL	MEM	0.7BH	R/W	Data memory row address pointer, low
IXL	MEM	0.7CH	R/W	Index register, low
RPH	MEM	0.7DH	R/W	General register pointer, high
RPL	MEM	0.7EH	R/W	General register pointer, low
PSW	MEM	0.7FH	R/W	Program status word
BCD	FLG	0.7EH.0	R/W	BCD flag
CMP	FLG	0.7FH.3	R/W	Compare flag
CY	FLG	0.7FH.2	R/W	Carry flag
Z	FLG	0.7FH.1	R/W	Zero flag
IXE	FLG	0.7FH.0	R/W	Index enable flag

Figure 21-1. Configuration of System Register

Address	74H				75H				76H				77H				78H				79H				7AH				7BH				7CH				7DH				7EH				7FH			
Name	Address register (AR)																Window register (WR)				Bank register (BANK)				Index register (IX) Data memory row address pointer (MP)												General register pointer (RP)							Program status word (PSWORD)				
Symbol	AR3				AR2				AR1				AR0				WR				BANK				IXH				IXM				IXL				RPH				RPL				PSW			
																									MPH				MPL																			
Bit	b_3	b_2	b_1	b_0	b_3	b_2	b_1	b_0	b_3	b_2	b_1	b_0	b_3	b_2	b_1	b_0	b_3	b_2	b_1	b_0	b_3	b_2	b_1	b_0	b_3	b_2	b_1	b_0	b_3	b_2	b_1	b_0	b_3	b_2	b_1	b_0	b_3	b_2	b_1	b_0	b_3	b_2	b_1	b_0	b_3	b_2	b_1	b_0
Data[Note 1]																										(IX)																						
	0	0	0	0	**Note 2**																0	0	0	0	MPE	0	0	0	0								0	0	0	0				BCD	CMP	CY	Z	IXE
	(AR)																				(BANK)					(MP)											(RP)											
Initial value at reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Undefined				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Notes 1. "0" in this field means that the bit is fixed to "0".

2. b_3 and b_2 of AR2 of the μPD17145 (A1) are fixed to 0. b_3 of AR2 of the μPD17147 (A1) is fixed to 0.

Data buffer (DBF)

Symbol Name	Attribute	Value	Read/Write	Description
DBF3	MEM	0.0CH	R/W	Bits 15 to 12 of DBF
DBF2	MEM	0.0DH	R/W	Bits 11 to 8 of DBF
DBF1	MEM	0.0EH	R/W	Bits 7 to 4 of DBF
DBF0	MEM	0.0FH	R/W	Bits 3 to 0 of DBF

Port register

Symbol Name	Attribute	Value	Read/Write	Description
P0A3	FLG	0.70H.3	R/W	Bit 3 of port 0A
P0A2	FLG	0.70H.2	R/W	Bit 2 of port 0A
P0A1	FLG	0.70H.1	R/W	Bit 1 of port 0A
P0A0	FLG	0.70H.0	R/W	Bit 0 of port 0A
P0B3	FLG	0.71H.3	R/W	Bit 3 of port 0B
P0B2	FLG	0.71H.2	R/W	Bit 2 of port 0B
P0B1	FLG	0.71H.1	R/W	Bit 1 of port 0B
P0B0	FLG	0.71H.0	R/W	Bit 0 of port 0B
P0C3	FLG	0.72H.3	R/W	Bit 3 of port 0C
P0C2	FLG	0.72H.2	R/W	Bit 2 of port 0C
P0C1	FLG	0.72H.1	R/W	Bit 1 of port 0C
P0C0	FLG	0.72H.0	R/W	Bit 0 of port 0C
P0D3	FLG	0.73H.3	R/W	Bit 3 of port 0D
P0D2	FLG	0.73H.2	R/W	Bit 2 of port 0D
P0D1	FLG	0.73H.1	R/W	Bit 1 of port 0D
P0D0	FLG	0.73H.0	R/W	Bit 0 of port 0D
P0E3	FLG	0.6EH.3	R/W	Bit 3 of port 0E
P0E2	FLG	0.6EH.2	R/W	Bit 2 of port 0E
P0E1	FLG	0.6EH.1	R/W	Bit 1 of port 0E
P0E0	FLG	0.6EH.0	R/W	Bit 0 of port 0E
P0F1	FLG	0.6FH.1	R	Bit 1 of port 0F
P0F0	FLG	0.6FH.0	R	Bit 0 of port 0F

Register file (control registers)

Symbol Name	Attribute	Value	Read/Write	Description
SP	MEM	0.81H	R/W	Stack pointer
SIOTS	FLG	0.82H.3	R/W	Serial interface start flag
SIOHIZ	FLG	0.82H.2	R/W	P0D$_1$/SO pin function select flag
SIOCK1	FLG	0.82H.1	R/W	Bit 1 of serial clock select flag
SIOCK0	FLG	0.82H.0	R/W	Bit 0 of serial clock select flag
WDTRES	FLG	0.83H.3	R/W	Watchdog timer reset flag
WDTEN	FLG	0.83H.0	R/W	Watchdog timer enable flag
TM1OSEL	FLG	0.8BH.3	R/W	P0D$_3$/$\overline{\mathrm{TM1OUT}}$ pin function select flag
SIOEN	FLG	0.8BH.0	R/W	Serial interface enable flag
P0EGPU	FLG	0.8CH.2	R/W	P0E group pull-up select flag (pull-up = 1)
P0BGPU	FLG	0.8CH.1	R/W	P0B group pull-up select flag (pull-up = 1)
P0AGPU	FLG	0.8CH.0	R/W	P0A group pull-up select flag (pull-up = 1)
P0DBPU3	FLG	0.8DH.3	R/W	P0D$_3$ pull-up select flag (pull-up = 1)
P0DBPU2	FLG	0.8DH.2	R/W	P0D$_2$ pull-up select flag (pull-up = 1)
P0DBPU1	FLG	0.8DH.1	R/W	P0D$_1$ pull-up select flag (pull-up = 1)
P0DBPU0	FLG	0.8DH.0	R/W	P0D$_0$ pull-up select flag (pull-up = 1)
INT	FLG	0.8FH.0	R	INT pin status flag
TM0EN	FLG	0.91H.3	R/W	Timer 0 enable flag
TM0RES	FLG	0.91H.2	R/W	Timer 0 reset flag
TM0CK1	FLG	0.91H.1	R/W	Bit 1 of timer 0 count pulse select flag
TM0CK0	FLG	0.91H.0	R/W	Bit 0 of timer 0 count pulse select flag
TM1EN	FLG	0.92H.3	R/W	Timer 1 enable flag
TM1RES	FLG	0.92H.2	R/W	Timer 1 reset flag
TM1CK1	FLG	0.92H.1	R/W	Bit 1 of timer 1 count pulse select flag
TM1CK0	FLG	0.92H.0	R/W	Bit 0 of timer 1 count pulse select flag
BTMISEL	FLG	0.93H.3	R/W	Basic interval timer interrupt request clock select flag
BTMRES	FLG	0.93H.2	R/W	Basic interval timer reset flag
BTMCK1	FLG	0.93H.1	R/W	Bit 1 of basic interval timer count pulse select flag
BTMCK0	FLG	0.93H.0	R/W	Bit 0 of basic interval timer count pulse select flag
P0C3IDI	FLG	0.9BH.3	R/W	P0C$_3$ input port disable flag (selects ADC$_3$/P0C$_3$ pin function)
P0C2IDI	FLG	0.9BH.2	R/W	P0C$_2$ input port disable flag (selects ADC$_2$/P0C$_2$ pin function)
P0C1IDI	FLG	0.9BH.1	R/W	P0C$_1$ input port disable flag (selects ADC$_1$/P0C$_1$ pin function)
P0C0IDI	FLG	0.9BH.0	R/W	P0C$_0$ input port disable flag (selects ADC$_0$/P0C$_0$ pin function)
P0CBIO3	FLG	0.9CH.3	R/W	P0C$_3$ input/output select flag (1 = output port)
P0CBIO2	FLG	0.9CH.2	R/W	P0C$_2$ input/output select flag (1 = output port)
P0CBIO1	FLG	0.9CH.1	R/W	P0C$_1$ input/output select flag (1 = output port)
P0CBIO0	FLG	0.9CH.0	R/W	P0C$_0$ input/output select flag (1 = output port)
IEGMD1	FLG	0.9FH.1	R/W	Bit 1 of INT pin edge detection select flag
IEGMD0	FLG	0.9FH.0	R/W	Bit 0 of INT pin edge detection select flag

Register file (control registers)

Symbol Name	Attribute	Value	Read/Write	Description
ADCSTRT	FLG	0.0A0H.0	R/W	A/D converter start flag (read: always “0”)
ADCSOFT	FLG	0.0A1H.3	R/W	A/D converter mode select flag (1 = single mode)
ADCCMP	FLG	0.0A1H.1	R	A/D converter comparator comparison result flag (valid only in single mode)
ADCEND	FLG	0.0A1H.0	R	A/D converter conversion end flag
ADCCH3	FLG	0.0A2H.3	R/W	Dummy flag
ADCCH2	FLG	0.0A2H.2	R/W	Dummy flag
ADCCH1	FLG	0.0A2H.1	R/W	Bit 1 of A/D converter channel select flag
ADCCH0	FLG	0.0A2H.0	R/W	Bit 0 of A/D converter channel select flag
P0DBIO3	FLG	0.0ABH.3	R/W	P0D$_3$ input/output select flag (1 = output port)
P0DBIO2	FLG	0.0ABH.2	R/W	P0D$_2$ input/output select flag (1 = output port)
P0DBIO1	FLG	0.0ABH.1	R/W	P0D$_1$ input/output select flag (1 = output port)
P0DBIO0	FLG	0.0ABH.0	R/W	P0D$_0$ input/output select flag (1 = output port)
P0EGIO	FLG	0.0ACH.2	R/W	P0E group input/output select flag (1 = all P0E as output port)
P0BGIO	FLG	0.0ACH.1	R/W	P0B group input/output select flag (1 = all P0B as output port)
P0AGIO	FLG	0.0ACH.0	R/W	P0A group input/output select flag (1 = all P0A as output port)
IPSIO	FLG	0.0AEH.0	R/W	Serial interface interrupt enable flag
IPBTM	FLG	0.0AFH.3	R/W	Basic interval timer interrupt enable flag
IPTM1	FLG	0.0AFH.2	R/W	Timer 1 interrupt enable flag
IPTM0	FLG	0.0AFH.1	R/W	Timer 0 interrupt enable flag
IP	FLG	0.0AFH.0	R/W	INT pin interrupt enable flag
IRQSIO	FLG	0.0BBH.0	R/W	Serial interface interrupt request flag
IRQBTM	FLG	0.0BCH.0	R/W	Basic interval timer interrupt request flag
IRQTM1	FLG	0.0BDH.0	R/W	Timer 1 interrupt request flag
IRQTM0	FLG	0.0BEH.0	R/W	Timer 0 interrupt request flag
IRQ	FLG	0.0BFH.0	R/W	INT pin interrupt request flag

Peripheral hardware registers

Symbol Name	Attribute	Value	Read/Write	Description
SIOSFR	DAT	01H	R/W	Peripheral address of shift register
TM0M	DAT	02H	W	Peripheral address of timer 0 modulo register
TM1M	DAT	03H	W	Peripheral address of timer 1 modulo register
ADCR	DAT	04H	R/W	Peripheral address of A/D converter data register
TM0TM1C	DAT	45H	R	Peripheral address of timer 0 timer 1 count register
AR	DAT	40H	R/W	Peripheral address of address register for GET/PUT/PUSH/CALL/BR/MOVT/INC instruction

Others

Symbol Name	Attribute	Value	Description
DBF	DAT	0FH	Fixed operand value of PUT, GET, and MOVT instructions
IX	DAT	01H	Fixed operand value of INC instruction

Figure 21-2. Configuration of Control Register

Column address Row address	Item	0				1				2				3				4				5				6				7			
0 (8)	Symbol					0	SP			SIOTS	SIOHIZ	SIOCK1	SIOCK0	WDTRES	0	0	WDTEN																
	At reset					0	1	0	1	0	0	0	0	0	0	0	0																
	Read/Write					R/W				R/W				R/W																			
1 (9)	Symbol					TM0EN	TM0RES	TM0CK1	TM0CK0	TM1EN	TM1RES	TM1CK1	TM1CK0	BTMISEL	BTMRES	BTMCK1	BTMCK0																
	At reset					0	0	0	0	1	0	0	0	0	0	0	0																
	Read/Write					R/W				R/W				R/W																			
2 (A)	Symbol	0	0	0	ADCSTRT	ADCSOFT	0	ADCCMP	ADCEND	ADCCH3	ADCCH2	ADCCH1	ADCCH0																				
	At reset	0	0	0	0	0	0	0	0	0	0	0	0																				
	Read/Write	R/W				R/W		R		R/W																							
3 (B)	Symbol																																
	At reset																																
	Read/Write																																

Remark ( ) is the address when the assembler (AS17K) is used.
All the flags of the control register are registered to the device file as assembler reserved words, and are convenient for program development.

Figure 21-2. Configuration of Control Register

8				9				A				B				C				D				E				F			
												TM1OSEL	0	0	SIOEN	0	P0EGPU	P0BGPU	P0AGPU	P0DBPU3	P0DBPU2	P0DBPU1	P0DBPU0					0	0	0	INT
												0	0	0	0	0	0	0	0	0	0	0	0					0	0	0	Note
												R/W				R/W				R/W								R			
												P0C3IDI	P0C2IDI	P0C1IDI	P0C0IDI	P0CBIO3	P0CBIO2	P0CBIO1	P0CBIO0									0	0	IEGMD1	IEGMD0
												0	0	0	0	0	0	0	0									0	0	0	0
												R/W				R/W												R/W			
												P0DBIO3	P0DBIO2	P0DBIO1	P0DBIO0	0	P0EGIO	P0BGIO	P0AGIO					0	0	0	IPSIO	IPBTM	IPTM1	IPTM0	IP
												0	0	0	0	0	0	0	0					0	0	0	0	0	0	0	0
												R/W				R/W								R/W				R/W			
												0	0	0	IRQSIO	0	0	0	IRQBTM	0	0	0	IRQTM1	0	0	0	IRQTM0	0	0	0	IRQ
												0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0
												R/W				R/W				R/W				R/W				R/W			

Note INT flag differs depending on the status of the INT pin at that time.

22. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_a = 25 °C)

Parameter	Symbol	Condition		Ratings	Unit
Supply voltage	V_{DD}			–0.3 to +7.0	V
A/D converter reference voltage	V_{REF}			–0.3 to V_{DD} + 0.3	V
Input voltage	V_I	P0A, P0B, P0C, P0D, P0E, P0F, INT, $\overline{\text{RESET}}$, X_{IN}		–0.3 to V_{DD} + 0.3	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
High-level output current	I_{OH} Note	Per P0A, P0B, or P0C	Peak value	–15	mA
			Effective value	–7.5	mA
		Total of P0A, P0B, and P0C	Peak value	–30	mA
			Effective value	–15	mA
Low-level output current	I_{OL} Note	Per P0A, P0B, or P0C	Peak value	15	mA
			Effective value	7.5	mA
		Per P0D or P0E	Peak value	30	mA
			Effective value	15	mA
		Total of P0A, P0B, P0C, P0D, and P0E	Peak value	100	mA
			Effective value	50	mA
Operating temperature	T_{opt}			–40 to +110	°C
Storage temperature	T_{stg}			–65 to +150	°C
Power dissipation	P_d	T_a = 85 °C	28-pin plastic shrink DIP	140	mW
			28-pin plastic SOP	85	mW

Note [Effective value] = [Peak value] × $\sqrt{\text{Duty}}$

Caution If the value of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. The absolute maximum ratings are the values exceeding which may physically damage the product. Be sure to use the product with these values not exceeded.

Recommended Supply Voltage Range (T_a = –40 to +110 °C)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	CPU (other than A/D converter and POC circuit)	f_x = 400 kHz to 2 MHz	2.7		5.5	V
			f_x = 400 kHz to 4 MHz	3.6		5.5	V
			f_x = 400 kHz to 8 MHz	4.5		5.5	V
		A/D converter	Absolute accuracy: ±1.5LSB, 2.5 V ≤ V_{REF} ≤ V_{DD}	4.0		5.5	V
		POC circuit (mask option)	f_x = 400 kHz to 4 MHz	4.5		5.5	V

DC Characteristics (V_{DD} = 2.7 to 5.5 V, T_a = –40 to +110 °C)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P0A, P0B, P0C, P0D, P0E, P0F		$0.7V_{DD}$		V_{DD}	V
	V_{IH2}	$\overline{\text{RESET}}$, $\overline{\text{SCK}}$, SI, INT		$0.8V_{DD}$		V_{DD}	V
	V_{IH3}	X_{IN}		$V_{DD} – 0.5$		V_{DD}	V
Input voltage, low	V_{IL1}	P0A, P0B, P0C, P0D, P0E, P0F		0		$0.3V_{DD}$	V
	V_{IL2}	$\overline{\text{RESET}}$, $\overline{\text{SCK}}$, SI, INT		0		$0.2V_{DD}$	V
	V_{IL3}	X_{IN}		0		0.4	V
Output voltage, high	V_{OH}	P0A, P0B, P0C	$4.5 \le V_{DD} \le 5.5$ I_{OH} = –1.0 mA	$V_{DD} – 0.3$			V
			$2.7 \le V_{DD} < 4.5$ I_{OH} = –0.5 mA	$V_{DD} – 0.3$			V
Output voltage, low	V_{OL1}	P0A, P0B, P0C, P0D, P0E	$4.5 \le V_{DD} \le 5.5$ I_{OL} = 1.0 mA			0.3	V
			$2.7 \le V_{DD} < 4.5$ I_{OL} = 0.5 mA			0.3	V
	V_{OL2}	P0D, P0E I_{OL} = 15 mA	$4.5 \le V_{DD} \le 5.5$			1.0	V
			$2.7 \le V_{DD} < 4.5$			2.0	V
Input leakage current, high	I_{LIH}	P0A, P0B, P0C, P0D, P0E, P0F	$V_{IN} = V_{DD}$			5	μA
Input leakage current, low	I_{LIL}	P0A, P0B, P0C, P0D, P0E, P0F	V_{IN} = 0 V			–5	μA
Output leakage current, high	I_{LOH}	P0A, P0B, P0C, P0D, P0E	$V_{OUT} = V_{DD}$			5	μA
Output leakage current, low	I_{LOL}	P0A, P0B, P0C, P0D, P0E	V_{OUT} = 0 V			–5	μA
Internal pull-up resistor[Note 1]	R_{PULL}	P0A, P0B, P0E, P0F, $\overline{\text{RESET}}$, INT		50	100	250	kΩ
		P0D		3	10	30	kΩ
Supply current[Note 2]	I_{DD1}	Operation mode	f_x = 8.0 MHz V_{DD} = 5 V ± 10 %		2.0	4.5	mA
			f_x = 4.0 MHz V_{DD} = 5 V ± 10 %		1.4	3.3	mA
			f_x = 2.0 MHz V_{DD} = 3 V ± 10 %		0.5	1.5	mA
			f_x = 400 kHz V_{DD} = 5 V ± 10 %		0.9	1.7	mA
			f_x = 400 kHz V_{DD} = 3 V ± 10 %		0.3	1.0	mA
	I_{DD2}	HALT mode	f_x = 8.0 MHz V_{DD} = 5 V ± 10 %		1.0	2.0	mA
			f_x = 4.0 MHz V_{DD} = 5 V ± 10 %		0.9	1.9	mA
			f_x = 2.0 MHz V_{DD} = 3 V ± 10 %		0.3	1.0	mA
			f_x = 400 kHz V_{DD} = 5 V ± 10 %		0.7	1.5	mA
			f_x = 400 kHz V_{DD} = 3 V ± 10 %		0.3	0.9	mA
	I_{DD3}	STOP mode	V_{DD} = 5 V ± 10 %		3.0	30	μA
			V_{DD} = 3 V ± 10 %		2.0	30	μA

Notes 1. The pull-up resistors of P0F, $\overline{\text{RESET}}$, and INT are mask options.

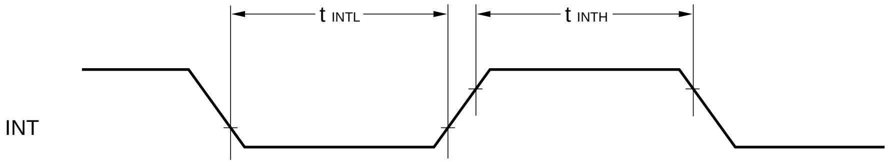
2. Excluding the current of the A/D converter and POC circuit, and the current flowing into the internal pull-up resistor.

AC Characteristics (V_{DD} = 2.7 to 5.5 V, T_a = –40 to +110 ˚C)

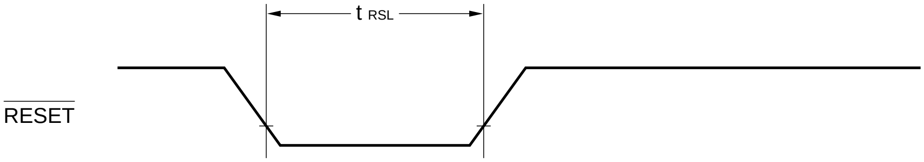
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CPU clock cycle time (instruction execution time)	t_{CY}	V_{DD} = 4.5 to 5.5 V	1.9		41	μs
		V_{DD} = 3.6 to 5.5 V	3.9		41	μs
			7.9		41	μs
INT input frequency (TM0 count clock input)	f_{INT}		0		400	kHz
INT high-, low-level width (external interrupt input)	t_{INTH}, t_{INTL}	V_{DD} = 4.5 to 5.5 V	10			μs
			50			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}	V_{DD} = 4.5 to 5.5 V	10			μs
			50			μs
$\overline{\text{RLS}}$ low-level width	t_{RLSL}	V_{DD} = 4.5 to 5.5 V	10			μs
			50			μs

Remark $t_{CY} = 16/f_X$ (f_X: system clock oscillation frequency)

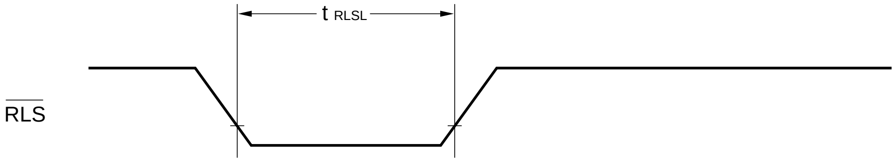
Interrupt input timing



$\overline{\text{RESET}}$ input timing



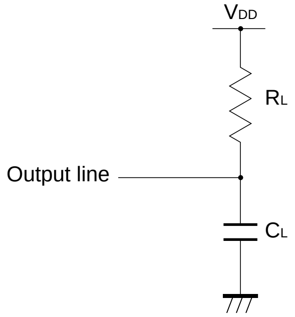
$\overline{\text{RLS}}$ input timing



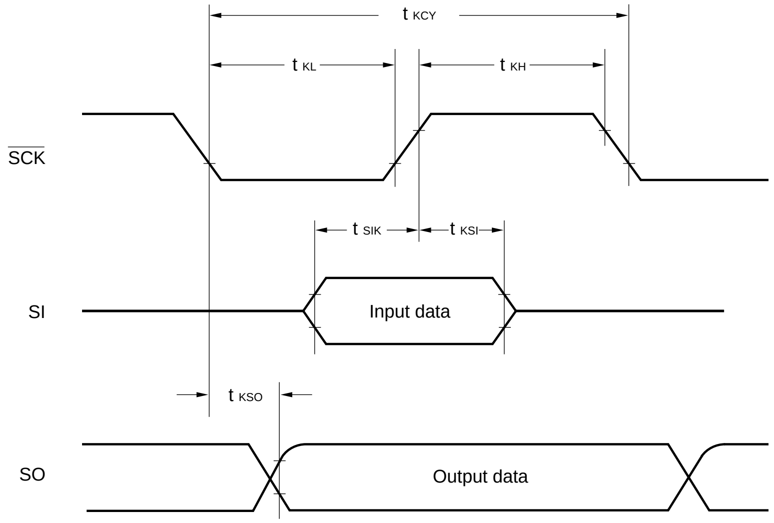
Serial transfer operation (V_{DD} = 2.7 to 5.5 V, T_a = –40 to +110 °C)

Parameter	Symbol	Condition			MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK}}$ cycle time	t_{KCY}	Input	V_{DD} = 4.5 to 5.5 V		2.0			μs
					10			μs
		Output	R_L = 1 kΩ,	V_{DD} = 4.5 to 5.5 V	2.0			μs
			C_L = 100 pF		8			μs
			Internal pull-up,	V_{DD} = 4.5 to 5.5 V	32			μs
			C_L = 100 pF		64			μs
$\overline{\text{SCK}}$ high-, low-level width	t_{KH}, t_{KL}	Input	V_{DD} = 4.5 to 5.5 V		1.0			μs
					5.0			μs
		Output	R_L = 1 kΩ,	V_{DD} = 4.5 to 5.5 V	t_{KCY}/2 – 0.6			μs
			C_L = 100 pF		t_{KCY}/2 – 1.2			μs
			Internal pull-up,	V_{DD} = 4.5 to 5.5 V	t_{KCY}/2 – 12			μs
			C_L = 100 pF		t_{KCY}/2 – 24			μs
SI setup time (to $\overline{\text{SCK}}$ ↑)	t_{SIK}				100			ns
SI hold time (from $\overline{\text{SCK}}$ ↑)	t_{KSI}				100			ns
SO output delay time from $\overline{\text{SCK}}$ ↓	t_{KSO}	R_L = 1 kΩ, C_L = 100 pF		V_{DD} = 4.5 to 5.5 V			0.8	μs
							1.4	μs
		Internal pull-up,		V_{DD} = 4.5 to 5.5 V			14	μs
		C_L = 100 pF					26	μs

Remark R_L: load resistance of output line
C_L: load capacitance of output line



Serial transfer timing



A/D Converter (V_{DD} = 4.0 to 5.5 V, T_a = –40 to +110 °C)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Absolute accuracy[Note 1]		$2.5\ V \leq V_{REF} \leq V_{DD}$			±1.5	LSB
Conversion time[Note 2]	t_{CONV}				25 t_{CY}	μs
Analog input voltage	V_{ADIN}		0		V_{REF}	V
Reference input voltage	V_{REF}		2.5		V_{DD}	V
A/D converter circuit current	I_{ADC}	When A/D converter operates		1.0	2.0	mA
V_{REF} pin current	I_{REF}			0.1	0.3	mA

Notes 1. Absolute accuracy excluding quantization error (±0.5LSB)

2. Time since a conversion start instruction has been executed until conversion ends (ADCEND = 1) (50 μs at 8 MHz).

Remark $t_{CY} = 16/f_x$ (f_x: system clock oscillation frequency)

POC Circuit (mask option[Note 1]) (V_{DD} = 2.7 to 5.5 V, T_a = –40 to +110 °C)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
POC detection voltage[Note 2]	V_{POC}		3.6	4.0	4.45	V
Supply voltage fall speed	t_{POCS}				0.08	V/ms
Reset detection pulse width	t_{SAMP}		1			ms
POC circuit current	I_{POC}			3.0	10	μA

Notes 1. The POC circuit can be used in an application circuit that operates at V_{DD} = 4.5 to 5.5 V, f_x = 400 kHz to 4 MHz.

2. This is the voltage at which the POC circuit clears its internal reset operation. The internal reset is cleared when $V_{POC} < V_{DD}$.

Oscillator Characteristics (V_{DD} = 2.7 to 5.5 V, T_a = –40 to +110 °C)

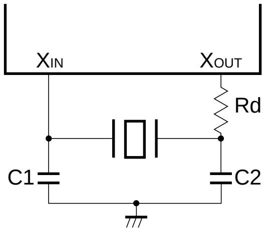
Resonator[Note]	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Ceramic resonator	Oscillation frequency		0.39		2.04	MHz
		V_{DD} = 3.6 to 5.5 V	0.39		4.08	MHz
		V_{DD} = 4.5 to 5.5 V	0.39		8.16	MHz

Note Do not use a resonator whose oscillation growth time exceeds 2 ms.

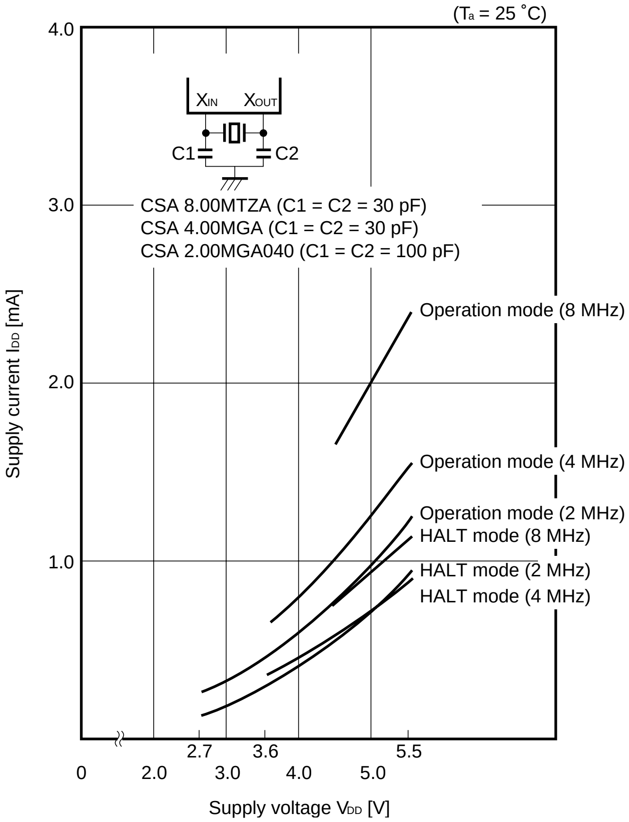
Recommended Ceramic Resonator (T_a = –40 to +110 °C)

Manufac-turer	Part Number	Recommended Constants			Operating Supply Voltage [V]		Remark
		C1 [pF]	C2 [pF]	Rd [kΩ]	MIN.	MAX.	
Murata Mfg. Co.	CSB400JA	220	220	5.6	2.7	5.5	For automotive electronics
	CSA2.00MGA040	100	100	0	2.7	5.5	
	CST2.00MGA040	Unnecessary (C-contained type)		0	2.7	5.5	
	CSA4.00MGA	30	30	0	3.6	5.5	
	CST4.00MGWA	Unnecessary (C-contained type)		0	3.6	5.5	
	CSA8.00MTZA	30	30	0	4.5	5.5	
	CST8.00MTWA	Unnecessary (C-contained type)		0	4.5	5.5	

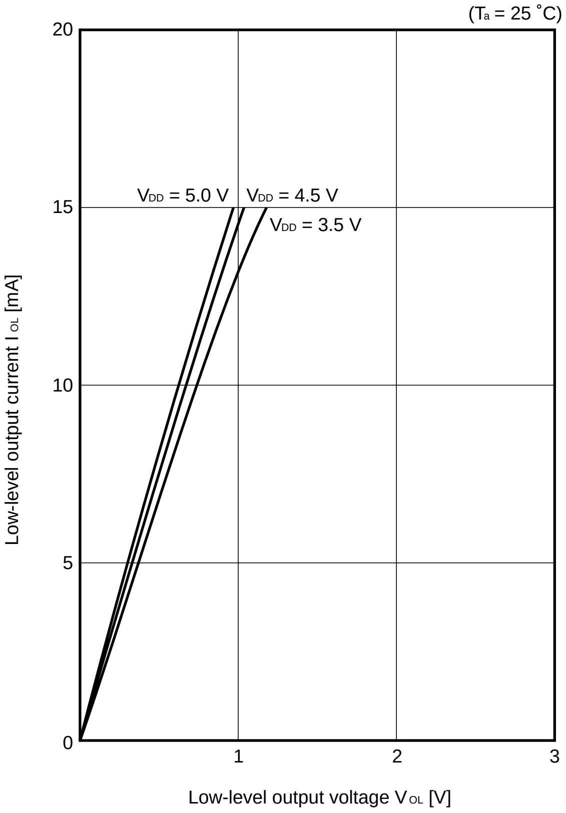
External Circuit Example



23. CHARACTERISTIC CURVE (REFERENCE VALUE)

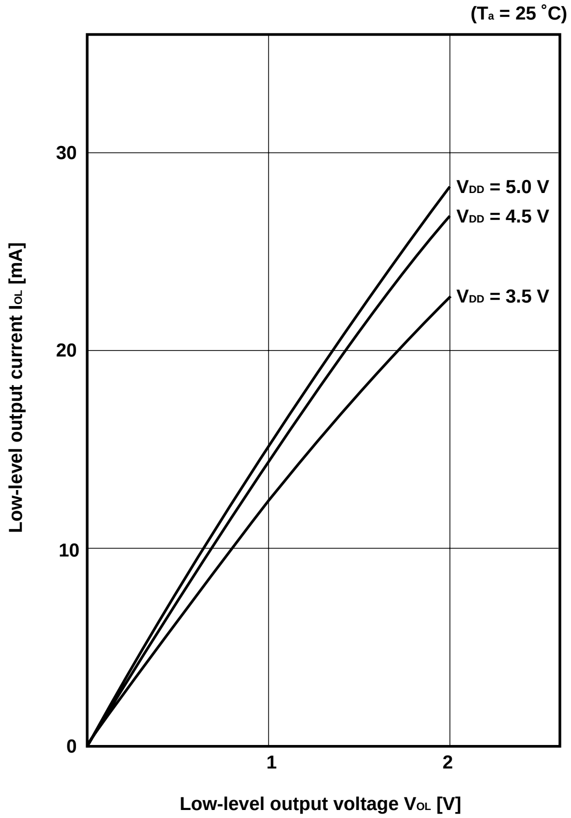


IOL vs. VOL Characteristic Example 1 (P0A, P0B, P0C)



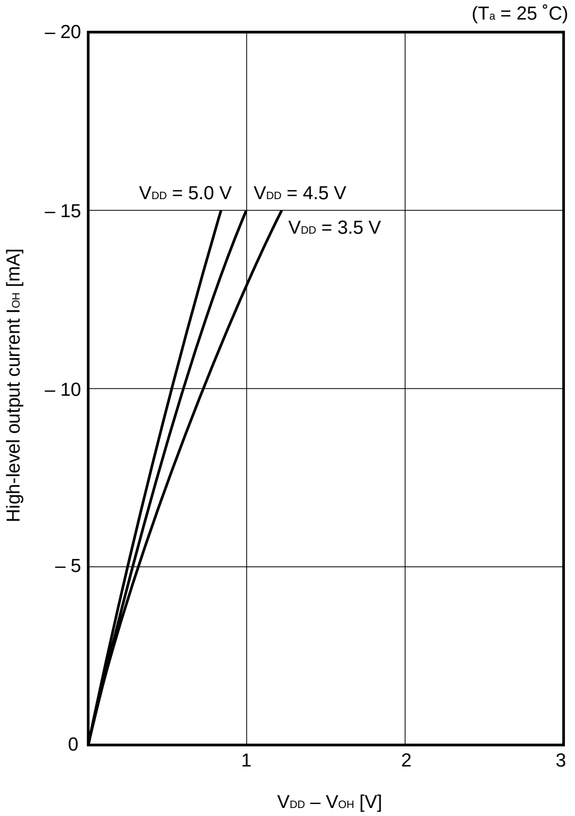
Caution The absolute maximum rating is 15 mA (peak value) per pin.

I_{OL} vs. V_{OL} Characteristics Example 2 (P0D, P0E)



Caution The absolute maximum rating is 30 mA (peak value) per pin.

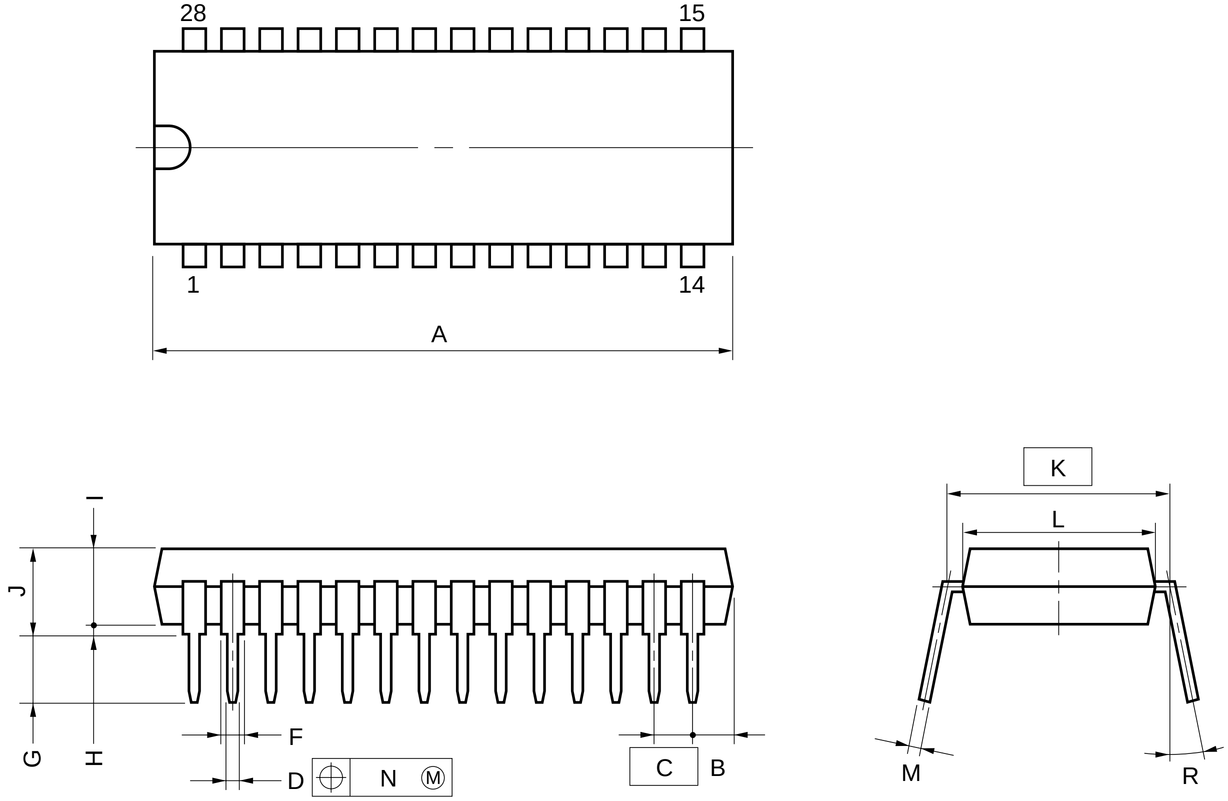
I_{OH} vs. (V_{DD} - V_{OH}) Characteristic Example



Caution The absolute maximum rating is –15 mA (peak value) per pin.

24. PACKAGE DRAWINGS

28 PIN PLASTIC SHRINK DIP (400 mil)



NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

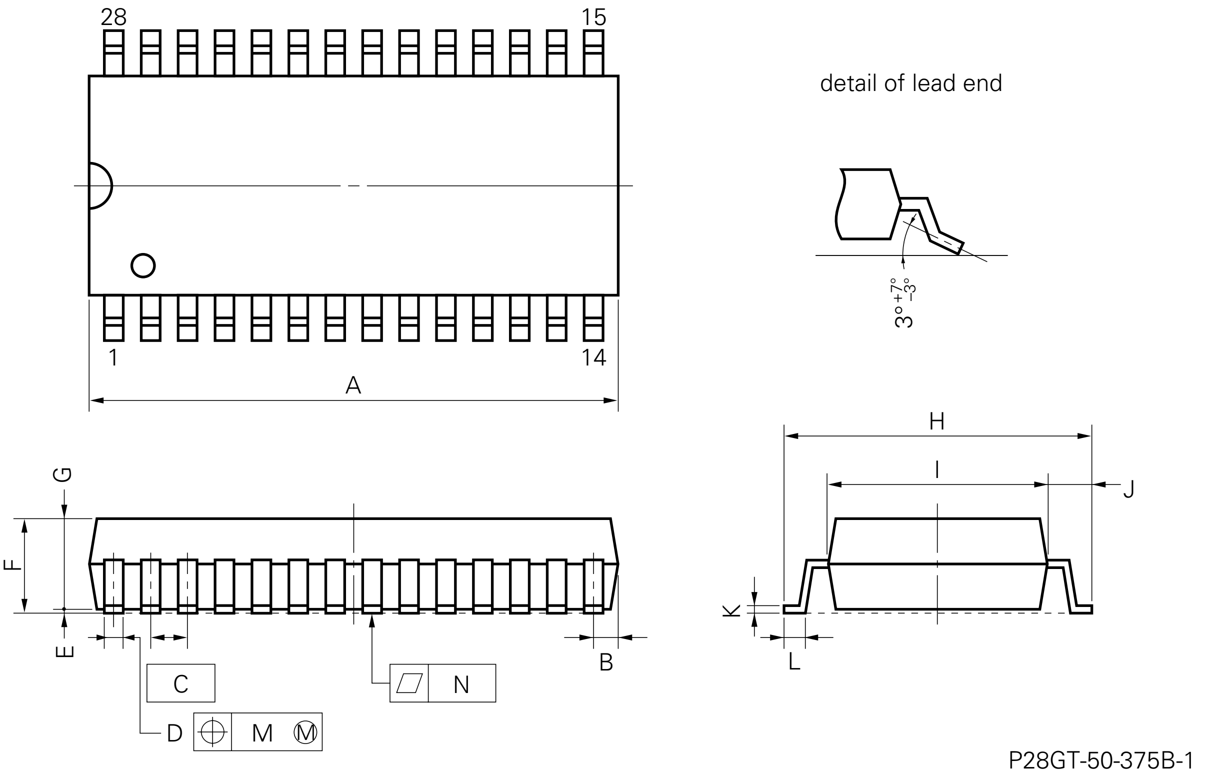
2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	28.46 MAX.	1.121 MAX.
B	2.67 MAX.	0.106 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	$0.020^{+0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	10.16 (T.P.)	0.400 (T.P.)
L	8.6	0.339
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

S28C-70-400B-1

Caution The ES model differs from the mass-produced model in terms of outline dimensions and materials. Refer to the drawing of the ES model.

28 PIN PLASTIC SOP (375 mil)



P28GT-50-375B-1

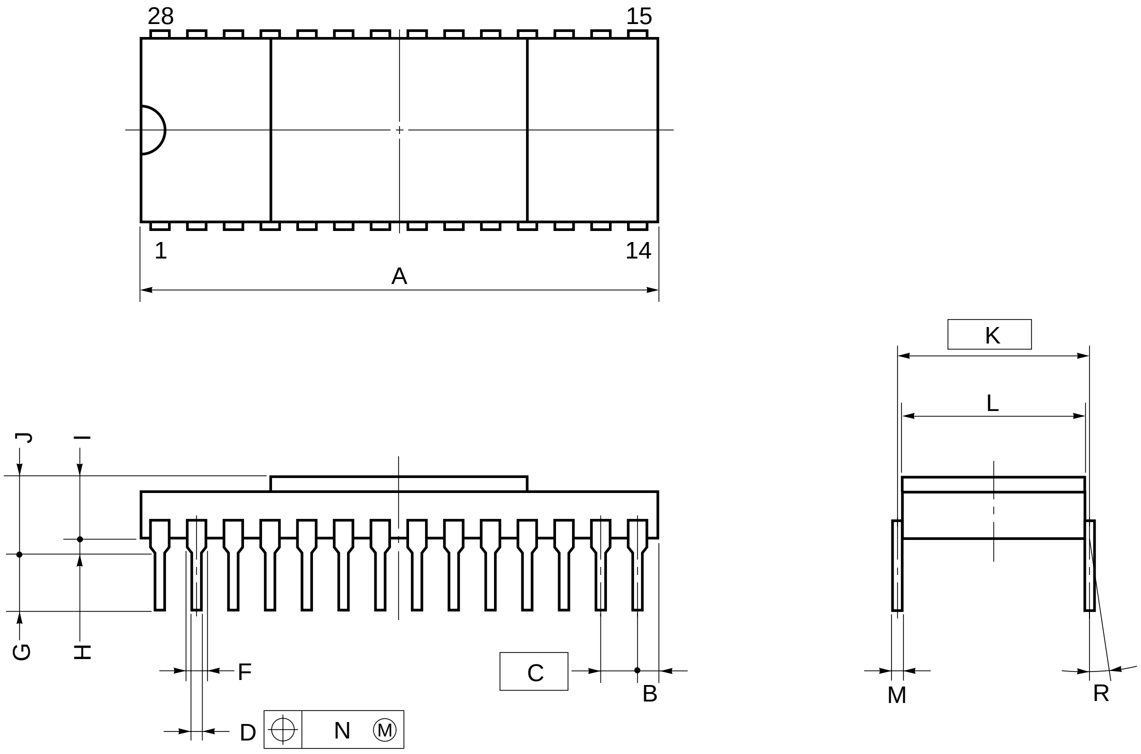
NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.2 MAX.	0.717 MAX.
B	0.845 MAX.	0.034 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.125±0.075	0.005±0.003
F	2.9 MAX.	0.115 MAX.
G	2.50±0.2	$0.098^{+0.009}_{-0.008}$
H	10.3±0.3	$0.406^{+0.012}_{-0.013}$
I	7.2±0.2	$0.283^{+0.009}_{-0.008}$
J	1.6±0.2	0.063±0.008
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005
N	0.10	0.004

Caution **The ES model differs from the mass-produced model in terms of outline dimension and materials. Refer to the drawing of the ES model.**

28 PIN CERAMIC SHRINK DIP (400 mil) (For ES)



NOTES

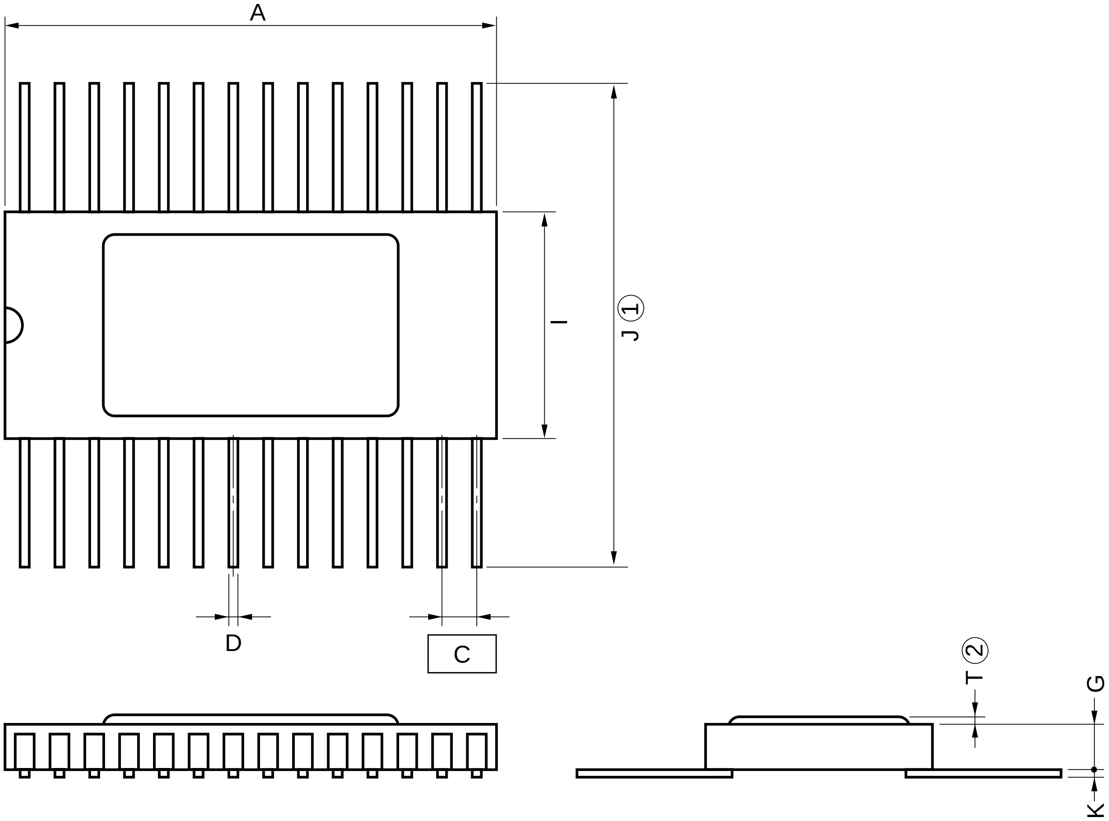
1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	28.0 MAX.	1.103 MAX.
B	5.1 MAX.	0.201 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.46±0.05	0.018±0.002
F	0.8 MIN.	0.031 MIN.
G	3.0±1.0	0.118±0.04
H	1.0 MIN.	0.039 MIN.
I	2.7	0.106
J	4.3 MAX.	0.170 MAX.
K	10.16 (T.P.)	0.400 (T.P.)
L	9.84	0.387
M	0.25±0.05	$0.010^{+0.002}_{-0.003}$
N	0.25	0.010
R	0~15°	0~15°

P28D-70-400B-1

28 PIN CERAMIC SOP (For ES)



NOTE

The lengths of leads (①) and the height of potting (②) are not to be specified because the lead cutting process and the potting process are not controlled.

ITEM	MILLIMETERS	INCHES
A	18.0±0.2	$0.709^{+0.008}_{-0.009}$
C	1.27 (T.P.)	0.05 (T.P.)
D	0.4±0.05	$0.016^{+0.002}_{-0.003}$
G	1.52±0.15	0.06±0.006
I	8.4±0.15	$0.331^{+0.006}_{-0.007}$
J	16.4	0.646
K	0.15±0.025	0.006±0.001
T	1.0	0.039

X28B-50B1

25. RECOMMENDED SOLDERING CONDITIONS

Solder this product under the following recommended conditions.

For details of the recommended soldering conditions, refer to Information Document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For the other soldering conditions and methods, consult NEC.

Table 25-1. Soldering Conditions of Surface Mount Type

μPD17145GT(A1)-×××: 28-pin plastic SOP (375 mil)
μPD17147GT(A1)-×××: 28-pin plastic SOP (375 mil)
μPD17149GT(A1)-×××: 28-pin plastic SOP (375 mil)

Soldering Method	Soldering Condition	Symbol of Recommended Condition
Infrared reflow	Package peak temperature: 235 °C, Time: 30 seconds max. (210 °C min.), Number of times: 2 max., Duration[Note]: 7 (after that, prebaking is necessary for 20 hours at 125 °C.) <Remarks> (1) Start second reflow after the device temperature that has risen because of the first reflow has fallen to room temperature. (2) Do not clean flux with water after the first reflow.	IR35-207-2
VPS	Package peak temperature: 215 °C, Time: 40 seconds max. (200 ˚C min.), Number of times: 2 max., Duration[Note]: 7 (after that, prebaking is necessary for 20 hours at 125 °C.) <Remarks> (1) Start second reflow after the device temperature that has risen because of the first reflow has fallen to room temperature. (2) Do not clean flux with water after the first reflow.	VP15-207-2
Pin partial heating	Pin temperature: 300 °C max., Time: 3 seconds max. (per side of device)	—

Note Number of storage days after the dry pack was opened. Storage conditions: 25 °C, 65 %RH max.

Caution Do not use two or more soldering methods in combination (except pin partial heating).

Table 25-2. Soldering Conditions of Insertion Type

μPD17145CT(A1)-×××: 28-pin plastic shrink DIP (400 mil)
μPD17147CT(A1)-×××: 28-pin plastic shrink DIP (400 mil)
μPD17149CT(A1)-×××: 28-pin plastic shrink DIP (400 mil)

Soldering Method	Soldering Condition
Wave soldering (pin only)	Solder bath temperature: 260 ˚C max., Time: 10 seconds max.
Pin partial heating	Pin temperature: 300 ˚C max., Time: 3 seconds max. (per side of pin)

Caution When performing wave soldering, exercise care that only the pins are wetted with solder and that no part of the package must be wetted.

APPENDIX A. FUNCTION COMPARISON BETWEEN μPD17145 SUBSERIES AND THE μPD17135A AND 17137A

		μPD17145	μPD17147	μPD17149	μPD17135A	μPD17137A
ROM		2 KB	4 KB	8 KB	2 KB	4 KB
RAM		110 × 4 bits			112 × 4 bits	
Stack		Address stack × 5 levels Interrupt stack × 3 levels				
Instruction execution time (clock, operating voltage)		2 μs (8 MHz, 4.5 to 5.5 V) 4 μs (4 MHz, 3.6 to 5.5 V) 8 μs (2 MHz, 2.7 to 5.5 V)			2 μs (8 MHz, 4.5 to 5.5 V) 4 μs (4 MHz, 2.7 to 5.5 V)	
I/O	CMOS I/O	12 (P0A, P0B, P0C)				
	Input	2 ($P0F_0$, $P0F_1$)			1 ($P1B_0$)	
	Sense input	1 (INT) Can be pulled up by mask option			1 (INT)	
	N-ch open-drain I/O	8 (P0D, P0E voltage: V_{DD}) P0D pull-up: software P0E pull-up: software			8 (P0D, P1A voltage: 9 V) P0D pull-up: mask option P1A pull-up: mask option	
Internal pull-up resistor		100 kΩ TYP. (except P0D) 10 kΩ TYP. (P0D)			100 kΩ TYP.	
A/D converter (operating voltage)		8 bits × 4 channels (V_{DD} = 4.0 to 5.5 V)			8 bits × 4 channels (V_{DD} = 4.5 to 5.5 V)	
	Reference voltage pin	V_{REF} (V_{REF} = 2.5 V to V_{DD})			None ($V_{REF} = V_{ADC} = V_{DD}$)	
Timer	8-bit (TM0, TM1)	2 (timer output: $\overline{\text{TM1OUT}}$) TM0 clock: system clock/512 system clock/64 system clock/16 INT TM1 clock: system clock/8192 system clock/128 system clock/16 TM0 count up			2 (timer output: $\overline{\text{TM0OUT}}$) TM0 clock: system clock/256 system clock/64 system clock/16 INT TM1 clock: system clock/1024 system clock/512 system clock/256 TM0 count up	
	Basic interval (BTM)	1 (also used as watchdog timer) Count clock: system clock/16384 system clock/4096 system clock/512 system clock/16			1 (also used as watchdog timer) Count clock: system clock/8192 system clock/4096 TM0 count up INT	
Interrupt	External	1			1 (with AC zero cross detection)	
	Internal	4 (TM0, TM1, BTM, SIO)				
SIO		1 (clocked 3-wire)				
	Output latch	Independent of $P0D_1$ latch			Shared with $P0D_1$ latch	
Standby function		HALT, STOP (can be released by $\overline{\text{RLS}}$ input pin)			HALT, STOP	

	μPD17145	μPD17147	μPD17149	μPD17135A	μPD17137A
Oscillation stabilization wait time	128 × 256 counts			512 × 256 counts	
POC function	Mask option			Internal	
Package	28-pin plastic SDIP (400 mil) 28-pin plastic SOP (375 mil)				
One-time PROM	μPD17P149			μPD17P137A	

Caution **The μPD17145 subseries is not pin-compatible with the μPD17135A and 17137A. The μPD17145 subseries does not include a product equivalent to the μPD17134A and 17136A (RC oscillation type). For the electrical specifications of each product, refer to the Data Sheet of the product.**

APPENDIX B. DEVELOPMENT TOOLS

The following development tools are available for developing programs for the μPD17145(A1), 17147(A1), and 17149(A1):

Hardware

Name	Outline
In-circuit emulator IE-17K, IE-17K-ET[Note 1], EMU-17K[Note 2]	IE-17K, IE-17K-ET, and EMU-17K are in-circuit emulators that can be used with any products in the 17K series. IE-17K and IE-17K-ET are connected to PC-9800 series or IBM PC/AT™ as the host machine with RS-232-C. EMU-17K is inserted into an expansion slot of the PC-9800 series. These in-circuit emulators operate as the emulator for a device when used in combination with the dedicated system evaluation board (SE board) of the device. When man-machine interface, SIMPLEHOST™, is used a sophisticated debugging environment can be realized. EMU-17K also has a function that allows real-time monitoring of the contents of the data memory.
SE board (SE-17145)	SE-17145 is an SE board for the μPD17145 subseries. It can be used alone to evaluate the system, or in combination with an in-circuit emulator for debugging.
Emulation probe (EP-17K28CT)	EP-17K28CT is an emulation probe for the 17K series 28-pin shrink DIP (400 mil).
Emulation probe (EP-17K28GT)	EP-17K28GT is an emulation probe for the 17K series 28-pin SOP (375 mil). It connects the SE board and target system when used with EV-9500GT-28[Note 3].
Conversion adapter (EV-9500GT-28[Note 3])	EV-9500GT-28 is an adapter for the 28-pin SOP (375 mil). It is used to connect EP-17K28GT and target system.
PROM programmer[Note 4] (AF-9703, AF-9704, AF-9705 or AF-9706)	AF-9703, AF-9704, AF-9705, and AF-9706 are PROM programmers supporting the μPD17P149. By connecting programmer adapter AF-9808M to these programmers, the μPD17P149 can be programmed.
Programmer adapter[Note 4] (AF-9808M)	AF-9808M is an adapter used to program the μPD17P149, in combination with AF-9703, AF-9704, AF-9705, or AF-9706.

Notes 1. Low-cost model: external power supply type

2. This is a product of IC Corporation. For details, consult IC Corporation (Tokyo (03) 3447-3793).

3. Two EV-97500GT-28s are supplied with the EP-17K28GT. Five EV-9500GT-28s are separately available as a set.

4. These are products of Ando Electric Corporation. For details, consult Ando Electric Corporation (Tokyo (03) 3733-1151).

Software

Name	Outline	Host Machine	OS		Supply Media	Order Code
17K series assembler (AS17K)	AS17K is an assembler that can be used with any products in the 17K series. To develop the program of the μPD17145(A1), 17147(A1), and 17149(A1), the AS17K and a device file (AS17145, AS17147, or AS17149) are used in combination.	PC-9800 series	MS-DOS™		5"2HD	μS5A10AS17K
					3.5"2HD	μS5A13AS17K
		IBM PC/AT	PC DOS™		5"2HC	μS7B10AS17K
					3.5"2HC	μS7B13AS17K
Device file (AS17145, AS17147, AS17149)	AS17145, AS17147, and AS17149 are device files for the μPD17145(A1), 17147(A1), 17149(A1), and μPD17P149. They can be used in combination with the assembler for the 17K series (AS17K).	PC-9800 series	MS-DOS		5"2HD	μS5A10AS17145[Note]
					3.5"2HD	μS5A13AS17145[Note]
		IBM PC/AT	PC DOS		5"2HC	μS7B10AS17145[Note]
					3.5"2HC	μS7B13AS17145[Note]
Support software (SIMPLEHOST)	SIMPLEHOST is software that serves as man-machine interface on Windows™ when a program is developed by using an in-circuit emulator and a personal computer.	PC-9800 series	MS-DOS	Windows	5"2HD	μS5A10IE17K
					3.5"2HD	μS5A13IE17K
		IBM PC/AT	PC DOS		5"2HC	μS7B10IE17K
					3.5"2HC	μS7B13IE17K

Note μS××××AS17145 includes AS17145, AS17147, and AS17149.

Remark The version of the OS supported is as follows:

OS	Version
MS-DOS	Ver. 3.30 to Ver. 5.00A[Note]
PC DOS	Ver. 3.1 to Ver. 5.0[Note]
Windows	Ver. 3.0 to Ver. 3.1

Note Although MS-DOS Ver.5.00/5.00A and PC DOS Ver. 5.0 have a task swap function, this function cannot be used with this software.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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NEC devices are classified into the following three quality grades:
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Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

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The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books.
If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.
Anti-radioactive design is not implemented in this product.

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